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USING VARIATION DECOMPOSITION ANALYSIS TO DETERMINE THE EFFECT OF PROCESS ON WAFER- AND DIE-LEVEL UNIFORMITY IN OXIDE CMP

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ABSTRACT

Process optimization and control in oxide CMP require an understanding of the trade-offs in wafer and die-level uniformity, and their interaction, as functions of the polishing process conditions. We have examined the effects of down force and table speed, the two key factors affecting the polishing rate, on uniformity. Using variation decomposition analysis to decompose the measured variation into wafer, die, wafer-die interaction and residual components, we have determined that wafer-level variation can be improved by appropriate choice of process factors while die-level variation and the wafer-die interaction are largely process independent for the operating space examined. These results suggest the possibility of separate optimization of die-level pattern dependencies and the use of process parameter control for wafer-level uniformity.

I. INTRODUCTION

Chemical Mechanical Polishing (CMP) has emerged as a critical process for global and local planarization in silicon integrated circuit fabrication. Despite the relatively good uniformity achievable at the wafer level, large systematic and random die-level variations still remain [1]. A typical profile of a polished patterned wafer exhibits a smooth envelope trend, which corresponds to the wafer-level variation, and periodic variations of higher amplitude resulting from different polish rates of the die layout features. Process modeling and control of CMP require an understanding of how the polishing process conditions manifest themselves at both levels and how they interact. In this paper, we have examined the role of down force and table speed, the key factors affecting the removal rate, on both wafer- and die-level uniformity. The quantification of the process effects have been facilitated by our previously developed variation analysis technique which results in the decomposition of the raw variation into constituent wafer, die, wafer-die interaction, and residual components [2].

A brief review of variation decomposition analysis is presented in Section II. The decomposition techniques and the underlying assumptions are outlined. Measurement

requirements for effective decomposition and ways of interpreting decomposed data are also explained. The experimental methodology is presented in Section III. Details of the pre-CMP short-flow process, polishing conditions, and the measurements taken are described. Section IV outlines the key results found in this study. The conclusion as well as future research directions are finally presented in Section V.

II. VARIATION DECOMPOSITION

Variation decomposition assumes the total variation consists of four additive components: wafer-level, die-level, die-wafer interaction, and residual. Figure 1 is a flow diagram of the analysis technique. Wafer-level variation arises from equipment limitations and other macroscopic non-uniformities, and is obtained from our data-set using a down-sampled moving average analysis of the raw measurements [2]. The die-level variation captures the layout pattern dependency; such variation has die periodicity and is obtained using 2-D Fourier analysis of the wafer-level residual [2,3]. The wafer-die interaction accounts for wafer-edge or other effects where the underlying die pattern is perturbed as a function of the location of the die on the wafer; the interaction is also obtained here using a 2-D Fourier analysis. The residual component is assumed to consist of purely random sources of variation that remain after the above systematic variation components have been taken into account.

Measurement Requirements

Variation decomposition techniques may be used to analyze any spatial data measured across a wafer. The number of measurements and the sites to be measured per die depend on the effects to be studied. In the case of CMP, a good estimate of the die-level variation requires at least 5 measurements per die and all dies across a wafer should be probed to obtain the wafer-level variation and the wafer-die interaction. Increased measurements per die result in improved die-level variation estimates at the expense of measurement time. With the maximum number of sites dictated by measurement time, choice of sites to measure should be such that a wide range of patterns with different polish rates are measured. Measurement details for this work are given in Section III.

Evaluation of Decomposed Data

Variation decomposition will be applied to understand the effect of process conditions on the polish and planarization of both wafer and die topography. We wish to gain both qualitative and quantitative insight from the analysis. The extracted wafer-level variation gives qualitative information about the global polishing trends, and is quickly obtained by visual examination of three dimensional surface plots. The range and standard deviation of the topography height across a wafer provide quantitative indications of the effectiveness of the polishing process since the variation is low frequency. The die-level variation captures the effect of layout patterns, and insight is also gained by visual inspection of surface plots. The die-level range is a quantitative measure of the absolute differ-

ence in thickness due to patterns and is therefore an indication of the final step height and hence planarization. Die-level variation can be further modeled as a function of the layout factors for a detailed understanding [4]. The wafer-die interaction should be examined for large systematic variations but focus should be on minimizing the wafer- and die-level variations since these should improve the interaction term as well. The residual is random noise but should also be examined to ensure that it is random and low in amplitude, to gain confidence that the systematic sources of variation have indeed been taken into account.

III. EXPERIMENTAL METHODOLOGY

As a first attempt at understanding the role of process conditions on wafer- and die-level uniformity in CMP, we perform a Box-Wilson experiment with the down force and table speed as the factors of concern in combination with a simple single layer test mask. Prior to CMP, 6 inch wafers underwent a short-flow process consisting of 1 µm LPCVD TEOS deposition, metal deposition of 0.7 µm, pattern and etch, followed by deposition of 2 µm LPCVD TEOS. The mask used is shown in Figure 2. It consists of vias, varying pitch lines and constant pitch line. For practical purposes, it may be considered to consist of approximately 99% and 50% density regions. The maximum via size is 2x2 μm^2 while the via spacing is maintained at 20 µm in all directions. Metal is etched at the via sites thus the 99% density. The varying pitch lines have spaces ranging from 0.25 µm to 2 µm and the lines are constant at 20 µm with the pattern repeated across the region. The constant pitch region has lines and spaces of 20 µm.

The experimental polishing process conditions, as summarized in Figure 3 and Table 1, are selected to explore a relatively large range of the two process parameters: down force is varied from 4 to 8 psi, and table speed from 20 to 50 rpm. The final average thickness is maintained approximately constant by varying the polishing time for each process. Approximately of 1 µm of oxide was removed. For each process setting, wafers are also polished at 2/3 and 1/3 of the final polishing time to study planarization evolution with time. The polishing was done on a Strasbaugh 6SP machine and one head was used in this experiment. Table 2 is a summary of the polishing conditions common to all processes. The polishing pad was relatively new with 25 wafers polished before the experiment to “break in” the pad. The pad was conditioned after each wafer.

Figure 4 shows a schematic cross-section of the constant pitch region before CMP, and indicates the approximate locations for optical measurements. The metrology was done on an Opti Probe™ model 2600 from Therma Wave. Only over-metal regions were measured in the 99% density regions due to the resolution limitation of the metrology equipment. The thickness of the metal was added to the oxide thickness measured above metal, and the initial deposited LPCVD TEOS thickness was subtracted from the measured oxide thickness over silicon so that the reference was the bottom of the metal as shown. A total of 31 sites per die across all 32 dies were measured resulting in approximately 1000 observations per wafer.

IV. RESULTS AND DISCUSSION

The average topography thickness for all wafers before CMP as measured over metal regions was approximately 2.7 µm (2.0 µm of TEOS and 0.7 µm metal) with an average across-wafer range of 0.1 µm. The deposition profile was bowl shaped with thicker oxide deposited near the edges. Figure 5 shows the post CMP topography thickness for a representative wafer before decomposition. A smoothly varying envelop and the periodic variations, corresponding to the wafer and die-level variations respectively, are identifiable. The decomposed result is shown in Figure 6. The range of the die-level variation is larger than the wafer-level variation as is often the case in CMP [1]. The wafer-die interaction and the residual components have relatively small amplitudes. The process dependence of each component is detailed in the following paragraphs.

Process Dependence of Wafer-Level Uniformity

The wafer-level variation for Process B (high down force, high table speed) is shown in Figure 7 for the three polishing times. The polishing rate near the edges of the wafer is consistently faster than the center such that the initial bowl shaped deposition profile is transformed into a dome shape after 1/3 of the target polish time. The shape is then maintained for the subsequent polish. The depression at the center of the wafer-level topography thickness is due to the initial as-deposited thickness profile. Similar trends are observed for other process settings with differences arising only in the relative polish rates of the edges. It should be noted that the wafer-level variation is a strong function of process and does not necessarily follow the initial profile. Figure 8 is a comparison of the final wafer-level variation for the corner process conditions in the experimental design The edge polish rates decrease in order from B, D, C and finally A. The decrease in the removal rate at the center may be due to reduced slurry flow at the interior of the wafer which reduces the "chemical tooth" of the process. Increased stress at the wafer edge may also contribute to the fast polish at these regions.

Figure 9 shows the surface height range for all processes as a function of polish time. The range steadily increases with polish time except for Process A which has the largest range at 2/3 of its final polish time. Closer examination reveals that the Process A wafer polished at 2/3 of the final time has a larger than usual initial range before polish resulting in the anomaly of this data point. With this factor considered, low down force (Processes A and C) results in the lowest range over time. The standard deviation of the wafer-level variation, which is a good measure of uniformity, is shown in Figure 10. The two figures show that Process B has the worst wafer-level variation for the process space examined and that Process C is most robust. These results are consistent with previous reports [5] and correspond to the often observed trade-off between good uniformity and high throughput.

Process Dependence of Die-Level Uniformity

Figure 11 shows the time evolution of the die-level variation for Process C. Here we see that after 1/3 of the polish time, the 50% density region is nearly completely planarized; at 2/3 of the polish time, the features are completely eroded. The die then consists of 100% density regions separated by a global step height. The trend is similar for the entire process space examined. This indicates that down force and table speed in the examined range are not sufficient to improve the die-level uniformity.

Figure 12 shows the die-level variation for Processes B and D after final polish time. Visual comparison does not reveal significant process dependence on the die-level variation. Table 3 is a summary of the difference between the die-level variation for Process A and the other processes evaluated at all point on the die. A mean difference of zero (to 4 significant figures) is observed as expected from our extraction methods. The mean standard deviation of the difference is less than 2% of the minimum range of 0.38 μm for any process. This shows that the process dependence of the die-level variation is at most second order. Figure 13 shows the die-level variation range evolution with time for all processes and confirms a weak process dependence. The range is replotted in Figure 14 as a function of actual polish time to convey the throughput information. The weak process dependence of the die-level variation should be contrasted with the strong process dependence of the wafer-level variation.

Process Dependence of Wafer-Die Interaction and Residual

A typical wafer-die interaction surface is shown in Figure 6. The center dies have smaller interaction effect than those at the edge but we did not observe significant process dependence. We are investigating techniques for quantifying the effect of interaction terms but we believe a focus on wafer and die-level variations provide focal points for process calibration and optimization. The residuals for wafers polished to the target thickness were examined for all processes examined: a mean of 0 and mean standard deviation ranging between 0.011 μm and 0.012 μm from found.

V. CONCLUSION

We have shown that wafer-level variation is a strong function of down force and table speed while the die-level variation is largely process independent. This opens up opportunities for independent optimization of process to improve wafer-level variation without affecting die-level variation. Die pattern dependencies may need to be improved by modified techniques. Different pads and slurries are expected to have significant effects on the die-level variation and are being examined using similar approached. Variation decomposition of process experiments indicate that different mechanism may be attributed to the global and local polishing effects. This could enable hierarchical physical modeling of the CMP process. Further work will focus on examining a wider process space, developing new masks as well as new analysis techniques which will further contribute empirical and physical models for CMP.

ACKNOWLEDGEMENTS

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Figure 1. Variation Decomposition Flow Diagram

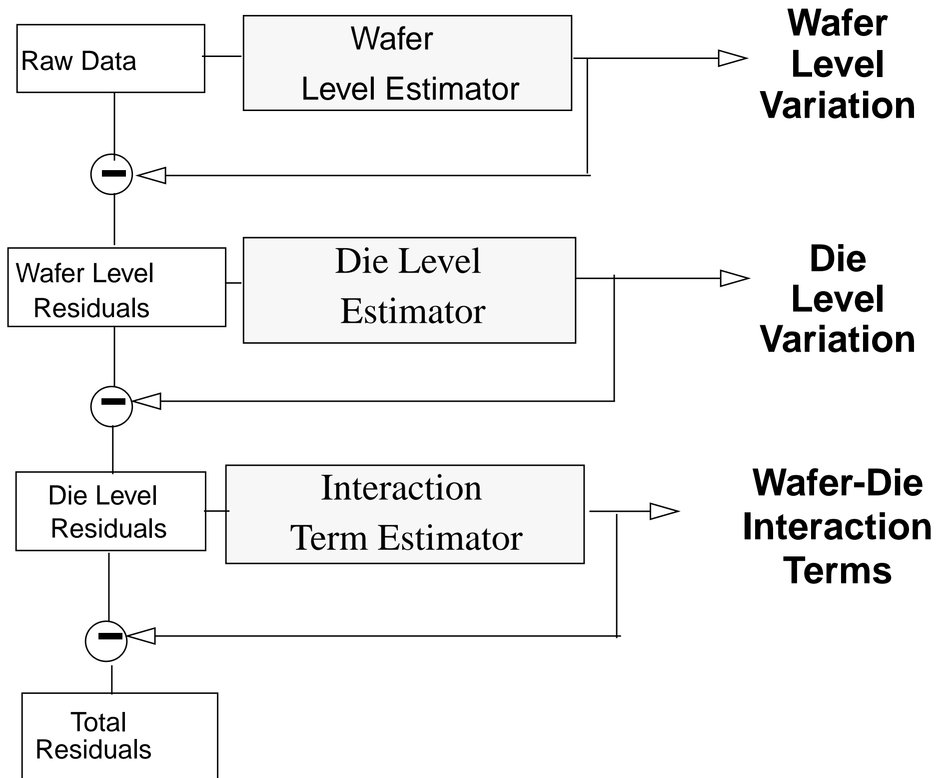


Figure 2. Mask Used for Process Experiment

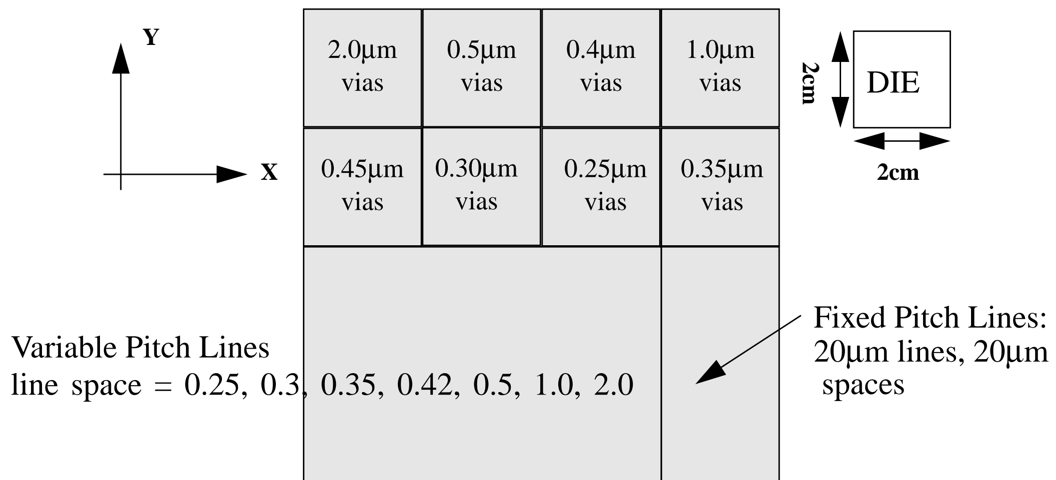


Figure 3. Process Conditions Explored

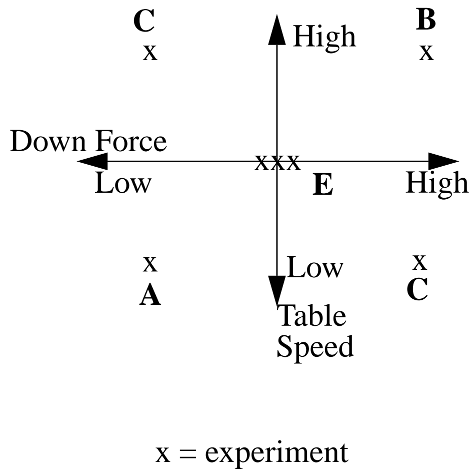


Table 1: Process Experiment

Process	Down Force (psi)	Table Speed (rpm)	Final Polish Time (s)	# Replicates
A (L,L)	4.0	20	460	1
B (H,H)	8.0	50	117	1
C (L,H)	4.0	50	252	1
D (H,L)	8.0	20	233	1
E (C,C)	5.5	35	220	3

Table 2: Common Polishing Conditions

Polishing Pad	IC 1400 (Grooved)
Spindle speed	20 rpm
Slurry type	SS 25 (Cabot Corp.)
Back Pressure	2 psi

Figure 4. Cross-section Before CMP

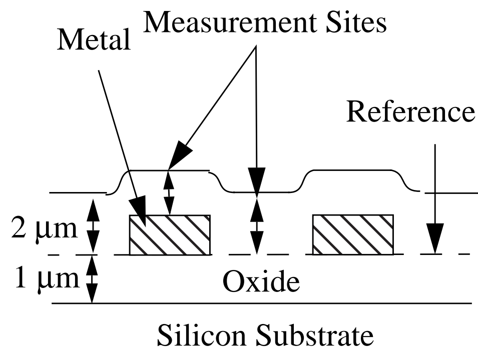


Figure 5. Raw Data for Process B after final Polish Time of 117 sec.

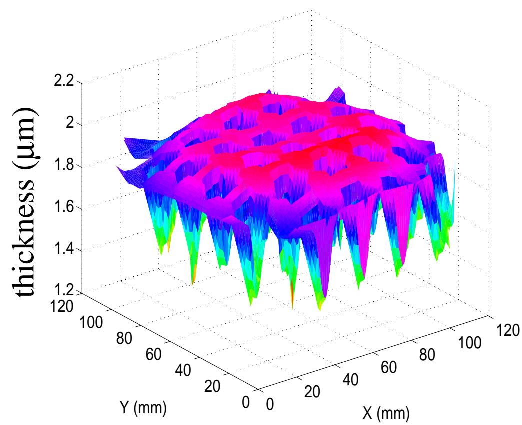


Figure 6. Decomposed Data for Process B after Polish Time of 117 sec.

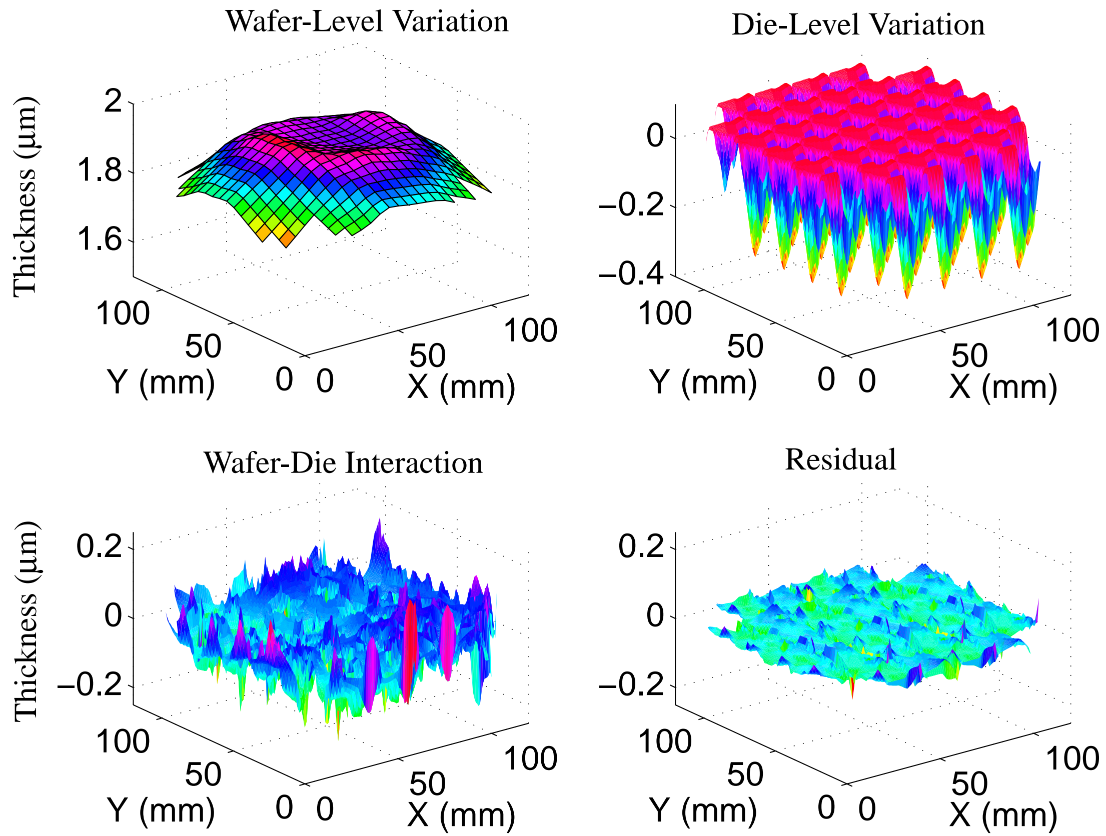


Figure 7. Wafer-Level Variation Evolution with Time for Process B

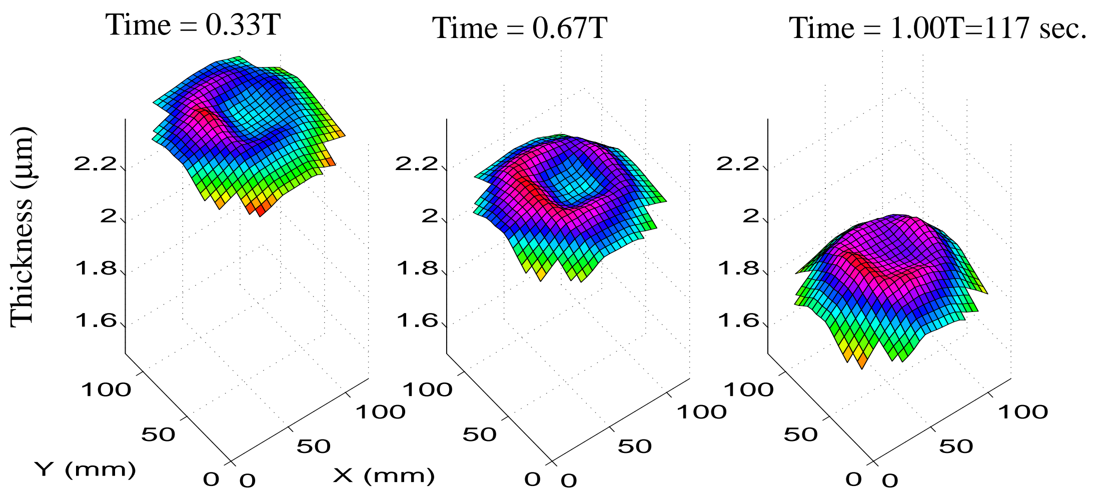


Figure 8. Comparison of Wafer-Level Variation for Processes at Final Polish Times

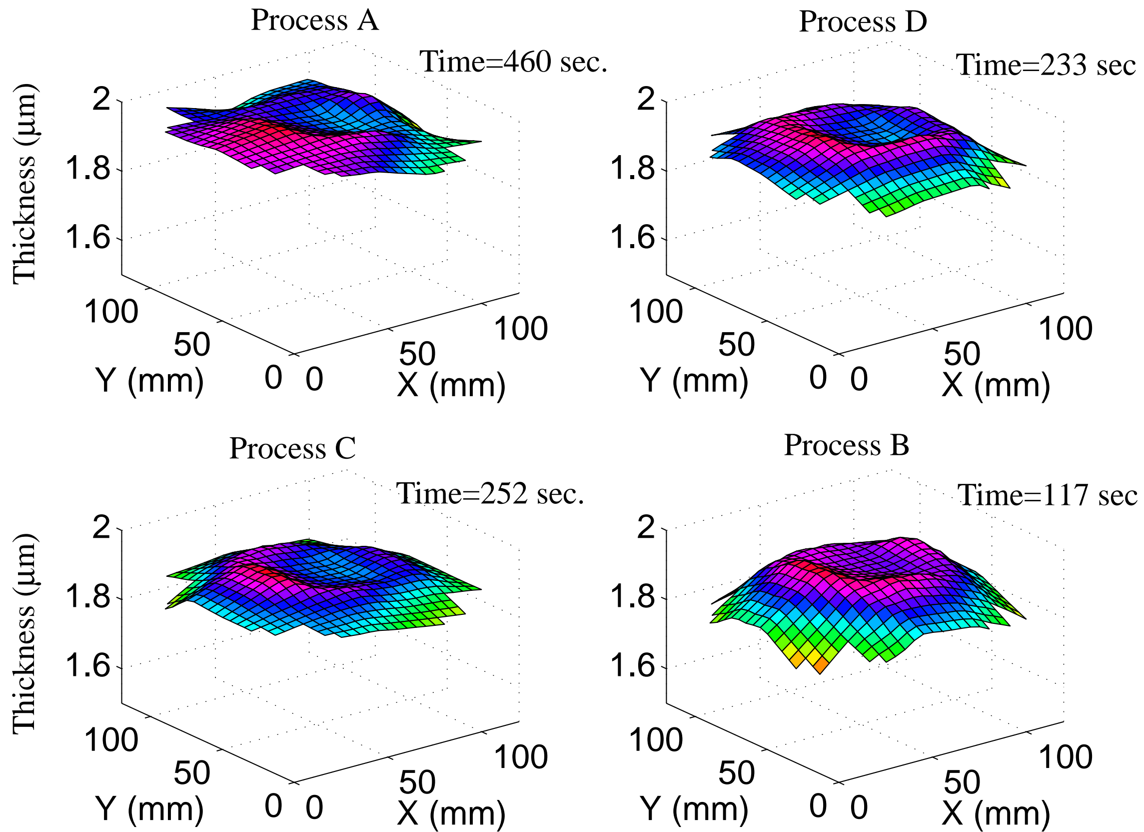


Figure 9. Wafer-Level Variation Range

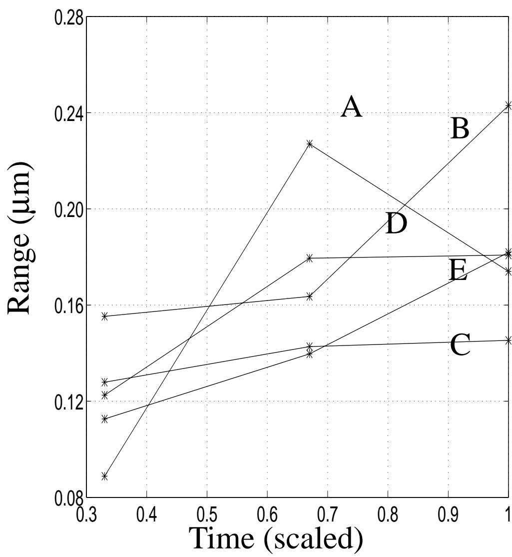


Figure 10. Wafer-Level Variation Standard Deviation

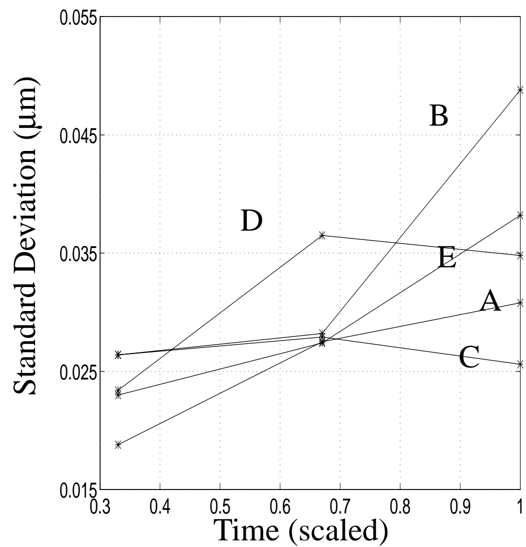


Figure 11. Die-Level Variation for Process C as a Function of Time

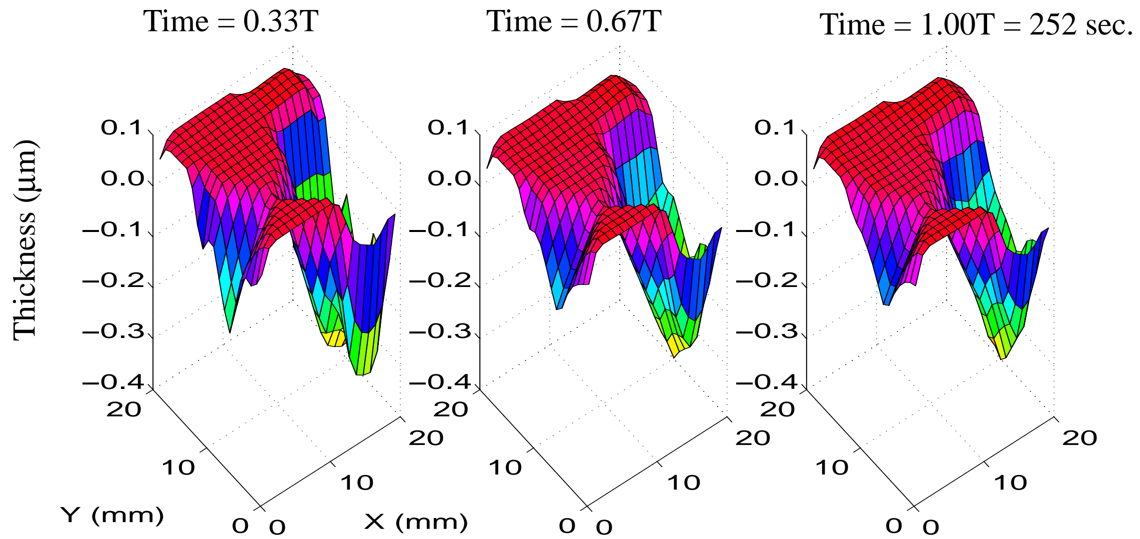
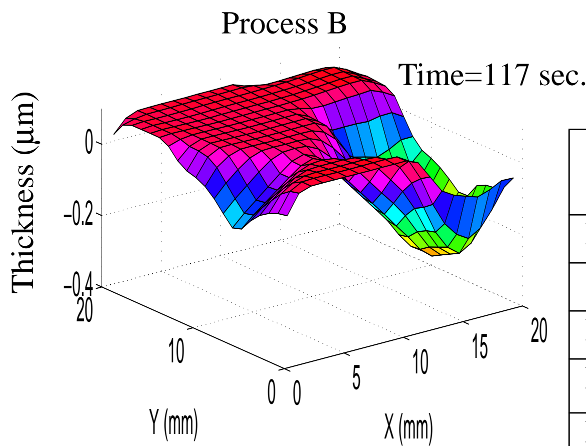


Figure 12. Comparison of Die-Level Variation across Process



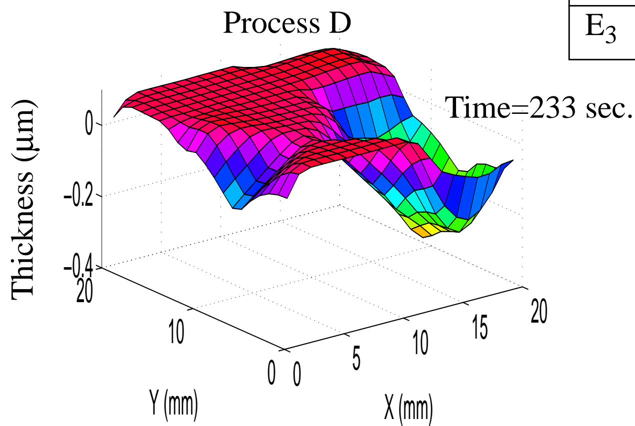


Table 3: Die-Level Variation Comparison

Process	Mean (µm)	Std (µm)	Range (µm)
B	0	0.0071	0.060
C	0	0.0084	0.084
D	0	0.0061	0.042
E_1	0	0.0061	0.058
E_2	0	0.0138	0.075
E_3	0	0.0062	0.041

Figure 13. Die-Level Variation Range with Scaled Time

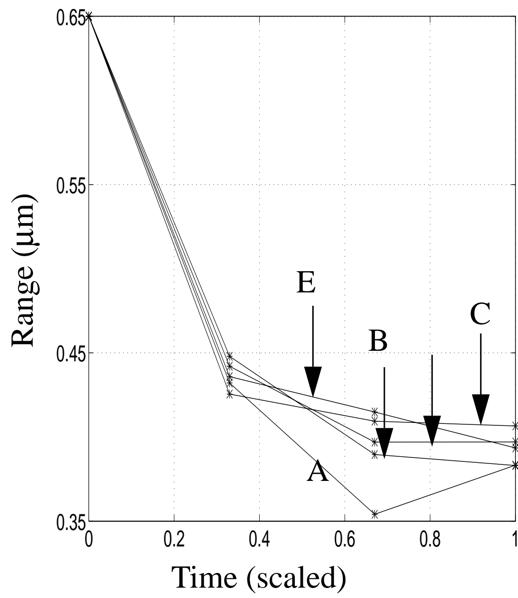


Figure 14. Die-Level Variation Range with Actual Time