Statistical metrology of interlevel dielectric thickness variation

Duane Boning, Tinaung Maung, James Chung
Microsystems Technology Laboratories
Massachusetts Institute of Technology, Cambridge, MA 02139

Keh-Jeng Chang, Soo-Young Oh, and Dirk Bartelink
Integrated Circuits Business Division
Hewlett Packard Co., Palo Alto, CA 94304

ABSTRACT

Statistical metrology seeks to assess the sources and magnitude of variation in semiconductor manufacturing. The methodology emphasizes electrical measurements resulting from short process flows, statistical design of experiments and analysis of data, and close coupling to technology computer aided design tools for the interpretation of data. In this paper, we apply statistical metrology to interlevel dielectric thickness variation. Capacitive test structures, in conjunction with resistive line width structures and two-dimensional capacitance simulations, are used to estimate ILD thickness for a variety of layout and process factors in a poly-metal BPSG planarization process. The methodology is successful in highlighting the key factors, including underlying structure line width spacing, and finger length that impact ILD thickness. Future work will examine other planarization processes, including chemical mechanical polishing.

Keywords: design for manufacturability, process variation, yield, interlevel dielectric thickness, statistical modeling, technology computer-aided design.

1. INTRODUCTION

The assessment and control of variation is of critical importance in semiconductor process development and manufacturing, particularly as device dimensions continue to shrink, levels of integration and die size increase, and the demand for performance rises. “Statistical metrology” is a methodology for the systematic evaluation and quantification of variation. The methodology emphasizes the use of electrical measurements in short flow processes, the application of statistical and numerical modeling tools and methods, and a focus on intradie variation in addition to other spatial or temporal variation sources. In this paper, we describe experimental work to apply statistical metrology to study the variation of interlevel dielectric (ILD) thickness in planarization processes.

We begin in Section 2 with an examination of the key elements of statistical metrology. In Section 3 we discuss interlevel dielectric thickness variation and its impact. The test structures and experimental design developed to study ILD thickness variation are described in Section 4. The methods for electrical measurement and conversion to ILD thickness are presented in Section 5, and the results of analysis in Section 6. Future work to extend to other planarization methods, particularly chemical mechanical polishing, is described in Section 7.

2. STATISTICAL METROLOGY

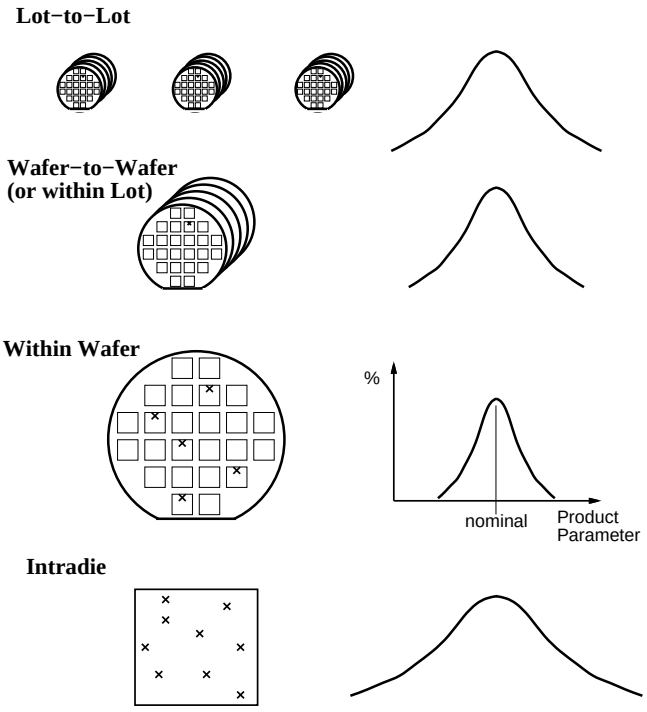
Statistical metrology is fundamentally a methodology to quantify variation and identify the sources of that variation. In this section, we first examine the scope of variation one encounters in semiconductor manufacturing, and then we describe key elements of the statistical metrology methodology.

2.1 Scope of Variation

Variation of structural and electrical parameters in semiconductor manufacturing appears with different scope or extent, as pictured in Fig. 1. Drifts, shifts, and noise in equipment and consumables give rise to lot-to-lot variation: the mean of some product parameter will vary from one lot to the next (in time) with some statistical distribution. Nonuniformity of processing within batch equipment, as well as additional equipment variation in single wafer processing, give rise to within lot, or wafer-to-wafer, variation.

Because the root causes of the variation at each scope are different, the distributions of one or the other may be larger. That is to say, one cannot assume that the "smaller" scope variation will in fact be smaller in magnitude than that of the surrounding scope. For example, lot-to-lot variation may be extremely well controlled in a polysilicon deposition process, but within lot variation (along the length of the tube) may still be quite large. Similarly, because different physical effects may cause within wafer nonuniformity than those causing wafer-to-wafer variation, it is necessary to separately assess each.

FIGURE 1. Scope of variation in semiconductor manufacturing.



An important implication is that intradie variation and within wafer variation can be caused by different physical effects. It is thus possible that intradie variation is *larger* than the within wafer variation. That is to say, the distribution of a parameter within one die may be larger than the distribution of the same structure (at the same location) on each die across the wafer. It is critical, therefor, to assess the size and impact of each variation source separately. While substantial effort has historically been devoted to measuring and monitoring wafer level variation, comparatively little attention has been paid to intradie variation. Zaghloul et al. studied variation in line width, including both intradie and wafer scale variation.[9] Tree-based classification was used to correlate end of line parameters with dedicated electrical test structures. Filtering of measurements was used to remove chip level effects (stepper distortions) and reveal wafer scale variation. Additional work focused on intradie line width variation has begun to appear.[2,4]

It must also be pointed out that variation has both systematic and random components. The "random" distribution of a product parameter typically includes largely systematic variation that one does not understand or cannot explain or model. For example, if systematic die effects (e.g. due to lens aberrations) are not understood, they will all be lumped together as random variation. The net effect of a successful statistical metrology methodology, in fact, is to transform as much "random" (or "statistical") variation as possible into well-understood and identifiable patterns of variation – to turn statistical noise into deterministic patterns.

2.2 Statistical Metrology Methodology

Statistical metrology is an approach to experimentally (1) quantify variation, and (2) identify the sources of variation for key semiconductor fabrication process modules. In order to accomplish this, the following elements are brought together.

First, we emphasize the electrical measurement of parameters in order to acquire the quantity of information necessary to draw meaningful conclusions. For example, the use of optical line width measurement of polysilicon critical dimension is possible, but can be extremely time consuming and demanding on the test infrastructure.[4] Electrical probing and test, on the other hand, is well suited to the acquisition of large volumes of data, including that at an intradie level.

Second, short flow process steps are used as much as possible. This is in contrast to the use of end-of line test structures for the measurement of cumulative variation and its impact on final device performance (which, of course, is also necessary). Rather, we seek to apply some of the same approaches in test structure and electrical measurement to early stages in process development, and aid in the assessment of variation during earlier process stages (e.g., during development of planarization, gate definition lithography, etc.).

Third, in this work we utilize the statistical design of experiments. As an extension to the traditional practice, during process development, of statistical design in the space of process factors, we also consider additional factors that may be responsible for systematic variation. In particular, this requires the design of experiments that study pattern and spatial dependencies. The statistical analysis of measurements resulting from these designs is also an important element of statistical metrology.

Finally, the close coupling to technology computer aided design (TCAD), or process and structure/device simulation tools is required. This is typical for end of line electrical characterization and coupling to compact transistor modeling. However, the application of TCAD to process step and module understanding is less common. Statistical metrology requires the use of TCAD tools in the analysis of the electrical measurements, and may also provide an opportunity to gather the data necessary to achieve well-tuned and calibrated TCAD tools.

In the rest of this paper, the application of statistical metrology to interlevel dielectric thickness variation, also discussed in Ref. 1, is expanded upon. Related work to study polysilicon critical dimensions resulting from lithography and etch processes is also driving the development of this methodology.[1,2]

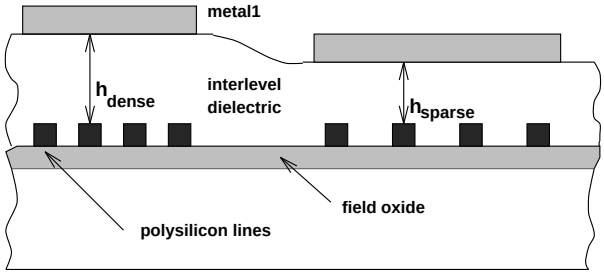
3. INTERLEVEL DIELECTRIC VARIATION

The elements of statistical metrology are being developed and applied to multilevel interconnect technology, specifically in characterizing planarization processes such as chemical mechanical polishing (CMP), spin on glass (SOG), and borophosphosilicate glass (BPSG) reflow. Circuit performance is increasingly limited by back-end processing, including etching, gap filling, and planarization. A key parameter in circuit design is the parasitic capacitance between lines in multiple interconnect layers. Not only is the nominal value of such capacitance important, the uncertainty in such capacitance introduced by structural variation can have a direct negative impact on critical circuit parameters (e.g. signal skew in nominally identical clock lines).

A good deal of recent work has focused on statistical modeling of circuit performance.[7] All of these depend fundamentally on estimated distributions of circuit elements. For example, Chow utilized circuit monitor test structures in circuit simulations to relate the distributions of transistor parameters to resulting analog circuit elements.[8] Such work is based on full circuit test structures, requires full flow fabrication, and neglects considerations of interconnect variation. Michaels and Ismail studied the impact of within wafer variation at the die level on circuit performance.[10]

The parameter of interest in this study is the variation in the dielectric thickness between lines in an underlying conductor and the overlying conducting layer, as illustrated in Fig. 2. While other parameters may also be of interest (e.g., the ILD thickness over unpatterned regions; the specifics of the geometry, such as curvature, around patterned features), the conductor-to-conductor ILD thickness has received most attention, since this has the most significant impact on final interconnect capacitance. We exercise the statistical metrology methodology described above to quantify the effectiveness and uniformity of planarizing ILD processes. Specifically, we describe (1) electrical test structures to acquire the volume of data necessary, (2) the statistical design of experiments to identify variation sources, and (3) the coupling to numerical TCAD tools to convert electrical measurements to ILD thickness information.

FIGURE 2. Interlevel dielectric thickness to be estimated via electrical measurements, illustrated for ILD dependence on density of underlying conductor lines.

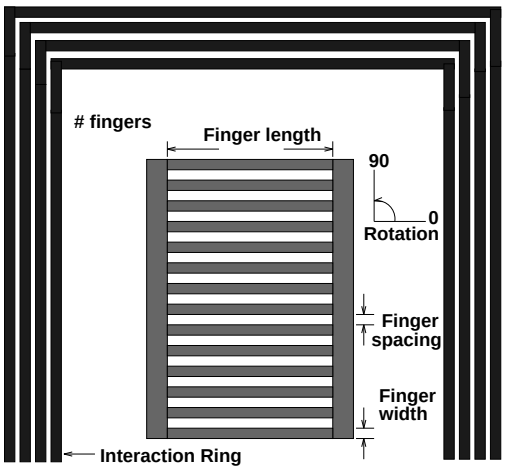


4. TEST STRUCTURES AND EXPERIMENTAL DESIGN

4.1 Test Structures

We use both electrical capacitance and line resistance measurements of test structures fabricated using a short flow process to infer ILD thickness information. The basic structure is a capacitor where the underlying electrode is a contacted, edge connected conductor grating of various dimensions and patterns, and the top electrode is a large area conductor plate covering the entire test structure. In the present experiments conducted at the MIT process facility, the materials system is specific to polysilicon and BPSG dielectric reflow, but the principles apply also to metal and CMP. A top-down view of a representative test structure is shown in Fig. 3.

FIGURE 3. Top view of capacitor test structure identifying layout factors in experimental design. The top conductor plate, not shown, covers only the inner ladder structure.



The test structure is designed to assess the impact of a set of possible factors on the ILD thickness. The layout factors to be examined using the test structure of Fig. 3 include the finger width, the spacing between fingers, the rotation angle of the fingers (vertical or horizontal), the number of fingers, the finger length, and lastly the presence or absence of an interaction ring. This last factor is to identify the distance over which structural processing interactions may take place, and complements the assessment of near-neighbor interactions arising between fingers.

4.2 Experimental Design

A two step experimental design strategy is used. The first step is a screening experiment to identify which layout and process factors and factor interactions have a significant impact on ILD thickness. We are using a 2^{6-1} fractional factorial experiment in the factors above (where the interaction distance is our half fraction). Besides these layout factors, other factors

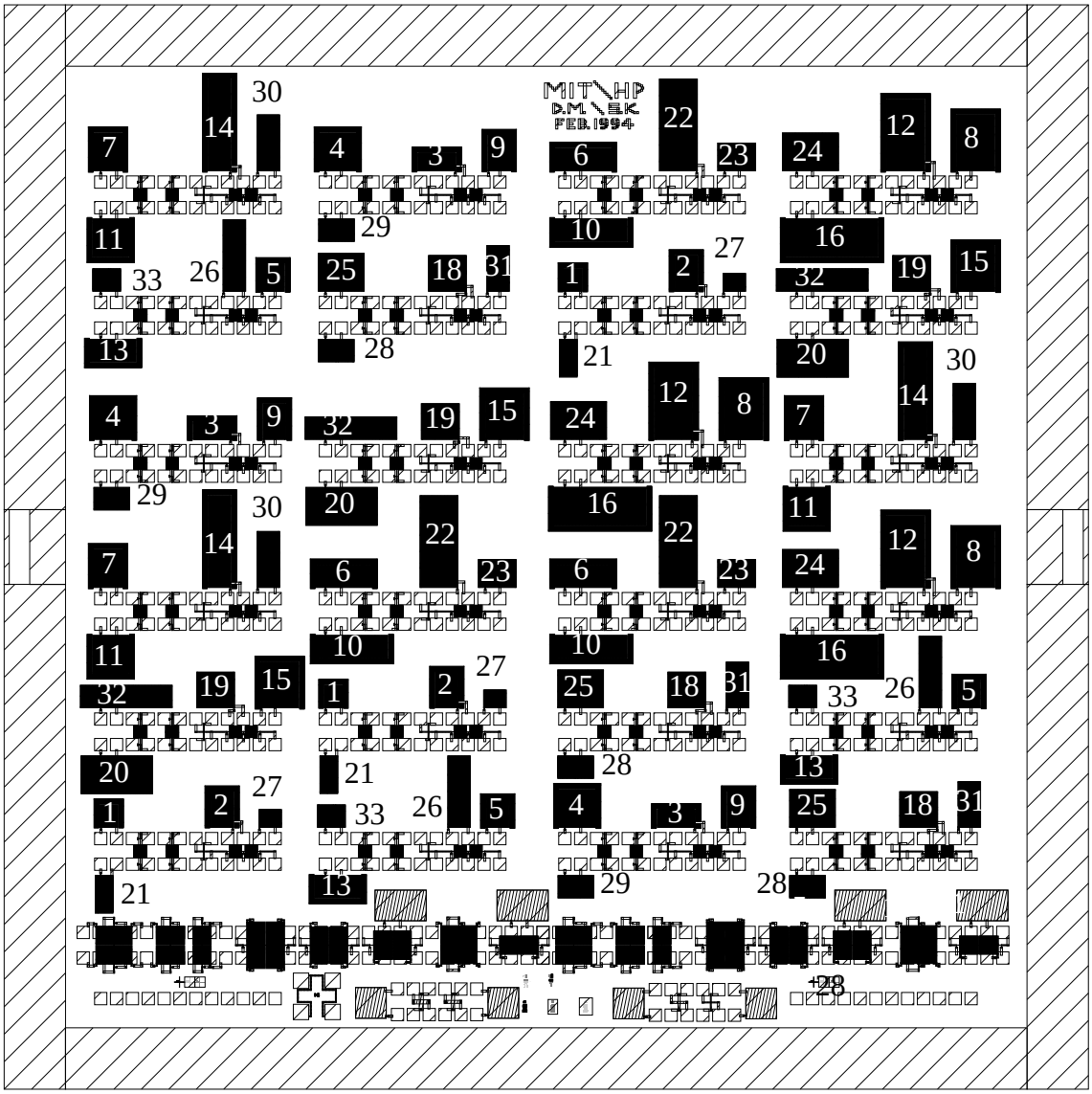
include the location of the test structure within the die and within the wafer, and process parameters in a process split. Based on the analysis of this experiment, the second step will be a design to more accurately quantify and model the contributions to variability.

The screening experiment uses two levels of each factor: finger widths are 1.5μm and 5.0μm, finger spacings are 2μm and 4μm, finger lengths are 200μm and 350μm, the number of fingers are 50 and 100, rotations are horizontal (0°) and vertical (90°), and an interaction ring is present at 25μm or absent. This design, summarized in Table 1, gives rise to 32 unique combinations of the layout factors and thus 32 different test structures. Within each 1cm x 1cm die, these test structures are replicated (and randomized) three times as shown in Fig. 4.

TABLE 1. ILD thickness variation test structure experimental design

Structure #	line width	spacing	length	# fingers	rotation	interaction
	+ = 5μm	+ = 4μm	+ = 350μm	+ = 100	+ = 90°	+ = present
	- = 1.5μm	- = 2μm	- = 200μm	- = 50	- = 0°	- = absent
1	+	+	+	+	+	+
2	+	+	+	+	-	-
3	+	+	+	-	+	-
4	+	+	+	-	-	+
5	+	+	-	+	+	-
6	+	+	-	+	-	+
7	+	+	-	-	+	+
8	+	+	-	-	-	-
9	+	-	+	+	+	-
10	+	-	+	+	-	+
11	+	-	+	-	+	+
12	+	-	+	-	-	-
13	+	-	-	+	+	+
14	+	-	-	+	-	-
15	+	-	-	-	+	-
16	+	-	-	-	-	+
17	-	+	+	+	+	-
18	-	+	+	+	-	+
19	-	+	+	-	+	+
20	-	+	+	-	-	-
21	-	+	-	+	+	+
22	-	+	-	+	-	-
23	-	+	-	-	+	-
24	-	+	-	-	-	+
25	-	-	+	+	+	+
26	-	-	+	+	-	-
27	-	-	+	-	+	-
28	-	-	+	-	-	+
29	-	-	-	+	+	-
30	-	-	-	+	-	+
31	-	-	-	-	+	+
32	-	-	-	-	-	-

FIGURE 4. Layout of test die showing replication and location of capacitive ILD thickness test structure.



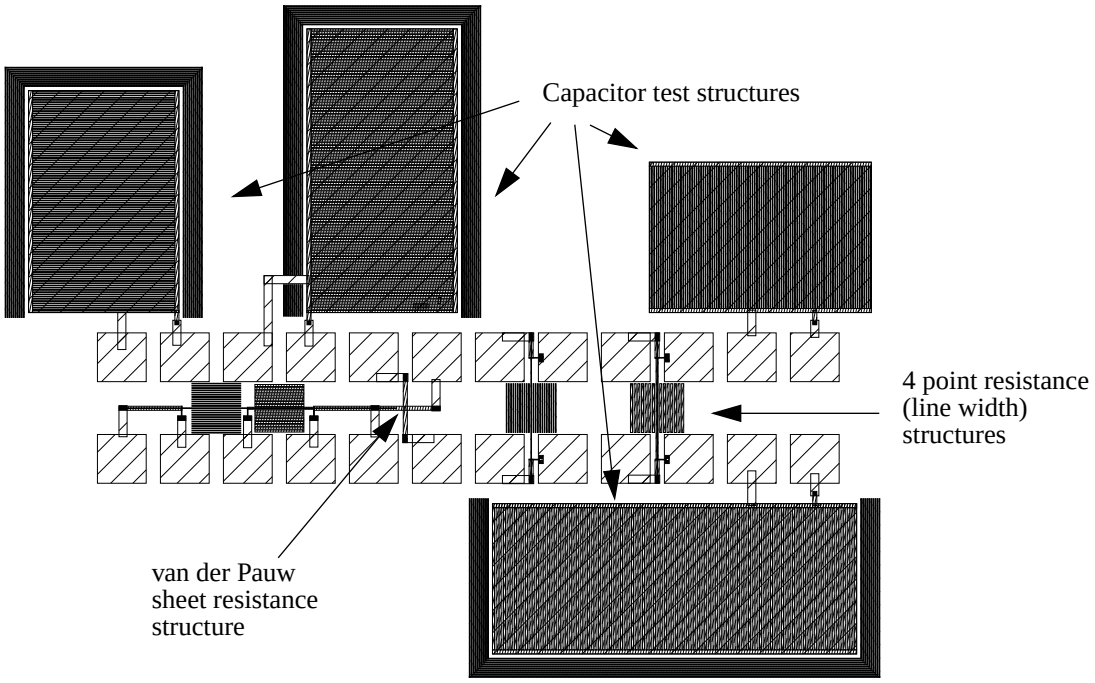
4.3 Subdie Design

The design of each electrically probe-able subdie is strongly influenced by the need to separate and identify individual sources of variation. We expect there to be, for example, an effect of the polysilicon line width on the ILD thickness. We also know from previous work[4,1] that the actual polysilicon line width will itself vary as a function of location (both intradie and across the wafer) and layout factors. Since the measured capacitance is linearly dependent on underlying line width and inversely related to ILD thickness, any errors in line width estimates will directly result in estimated ILD thickness errors. If we had previously characterized the variation of the poly lines (via statistical metrology), we could use this information to infer the capacitance structure line widths. The statistical metrology of lithography and etch have not yet been carried out for the process and equipment used in this experiment, however, so we must be careful to directly account for line width variation.

To compensate for the poly line width dependence, we add additional structures to each subdie as illustrated in Fig. 5. At the center of the subdie we use a van der Pauw structure to measure the sheet resistance of the polysilicon layer. We also place a single line resistor four point probe structure in the area between the pads. Each of these resistor structures is a smaller version of a corresponding large area capacitor structure in the same subdie; the line width and spacing of the resistor and sur-

rounding “dummy lines” match the experimental design width and spacing of its corresponding capacitor. In this way, we can electrically measure the line width of the resistive structures and use these measurements in the estimation of the poly line width of the nearby capacitive test structures.

FIGURE 5. Layout of subdie combining capacitive ILD thickness, resistive line width, and van der Pauw sheet resistance structures.



4.4 Process Flow

These same test structures can be applied to different planarization technologies, including dielectric layer reflow, spin-on glass, resist etchback, and chemical-mechanical polish approaches. In this paper, we report the first of these studies. The planarization process used in this study consists of a BPSG dielectric between polysilicon and metal1 layers. The process sequence is 5000 Å field oxide growth, 7000 Å polysilicon deposition and POCL doping, polysilicon patterning, BPSG deposition at a nominal thickness of 5000 Å or 6000 Å, contact pattern, metal deposition, and metal patterning.

5. ELECTRICAL MEASUREMENT AND THICKNESS CALCULATION

For each subdie in each die of the wafer, we collect capacitance, line resistance, and sheet resistivity data for all of the structures in the subdie. From this, we must estimate first the polysilicon line width of our test structures based on the resistance information, and second the ILD thickness based on the line width estimate and the capacitance information.

5.1 Line Width Estimation

A contour map showing representative sheet resistance variation across the wafer appears in Fig. 6, and across a die in Fig. 7. From this we see that, indeed, within a single die there is variation in the sheet resistance (in our process) that should be accounted for. Two methods of using the existing sheet resistance information are considered. First, we can assume that within any single subdie, the variation is small and apply the measured value directly to the line resistance test structures. Alternatively, we can attempt to compensate for subdie-level variation by (linearly) interpolating the sheet resistance values between the neighboring (horizontal) van der Pauw’s to estimate the sheet resistance value at each line width structure. In the analysis that follows, we have adopted the latter approach. Based on the electrical resistance measurement and estimated sheet resis-

tance, we calculate the line width for each drawn space/width combination in the subdie. We then use this as an estimate of the line width in the corresponding subdie capacitor structure.

FIGURE 6. Sheet resistance across the wafer.

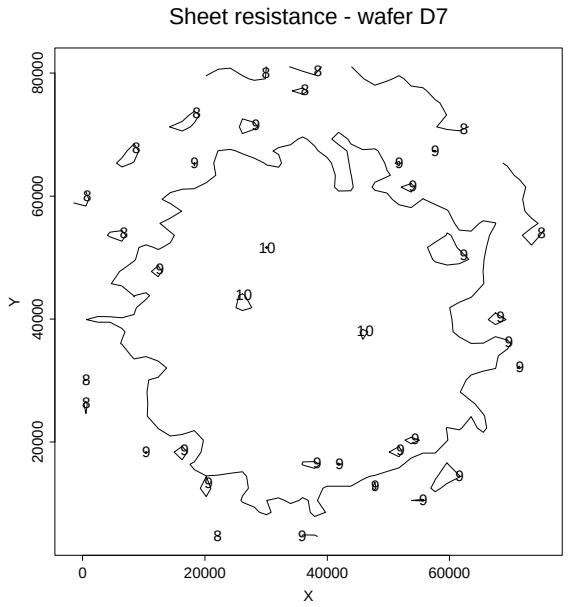
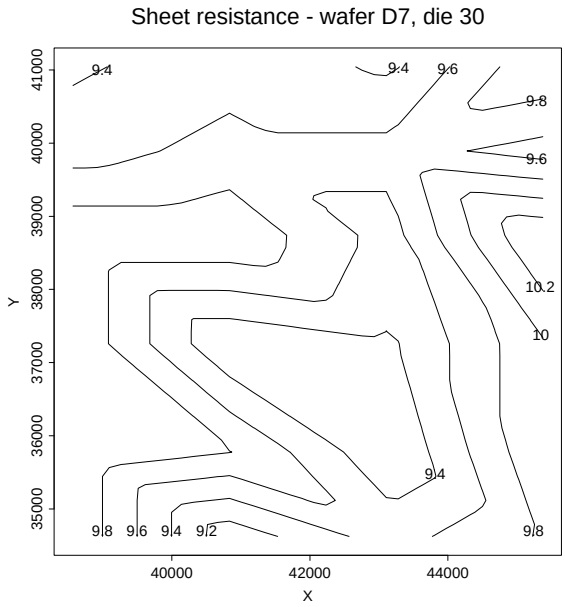


FIGURE 7. Sheet resistance across a single die.



5.2 Interlevel Dielectric Thickness Estimation

The second measurement conversion required is that of capacitance to ILD thickness. In this work, we follow the approach of Ref. 5, where precomputation of capacitance-width-thickness curves for each type of test structure is used. For each unique nominal (drawn) width/spacing combination in the experimental design (Table 1), two-dimensional Raphael[6] capacitance simulations are performed as shown in Fig. 8. A family of capacitance curves are generated by stepping through different line width variation (Δw) values, holding the pitch (line width + spacing) constant. For each Δw, a family of thicknesses (t_{ILD}) are stepped through and numerical simulations performed to generate structure-specific curves as pictured in Fig. 9. For any given capacitance measurement and line width, the ILD thickness is then estimated via two-dimensional linear interpolation as illustrated in Fig. 10.

FIGURE 8. Raphael ILD capacitance simulation structure. Reflecting boundary conditions are used at the outside edges of the half poly lines and through the middle of the silicon substrate.

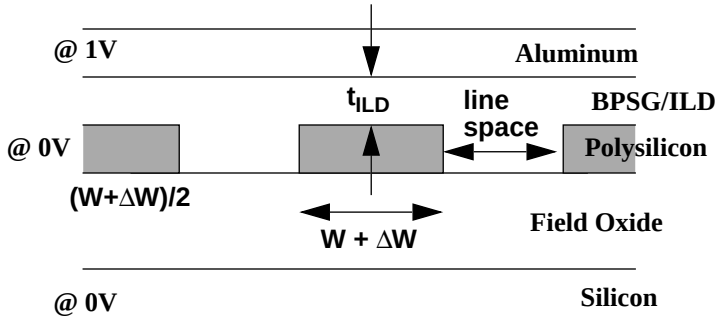


FIGURE 9. Simulated ILD thickness versus measured capacitance, as a function of polysilicon line width.

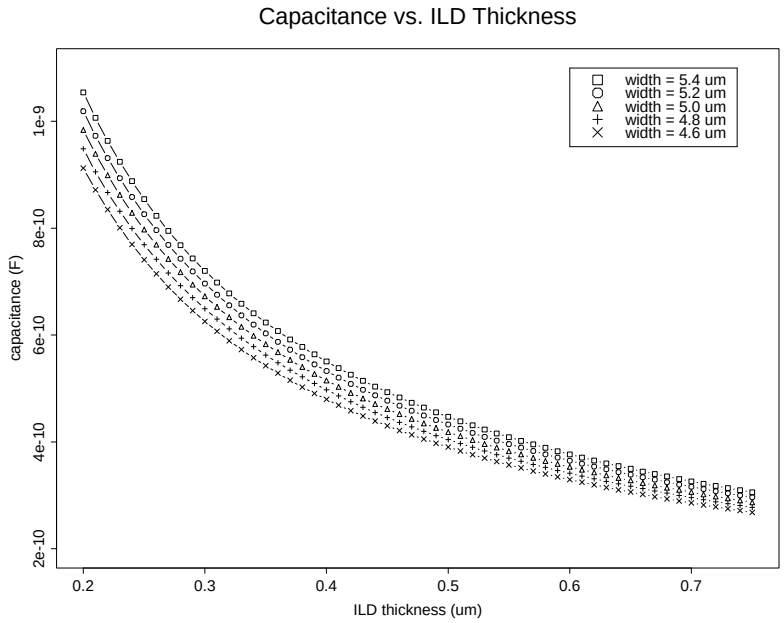
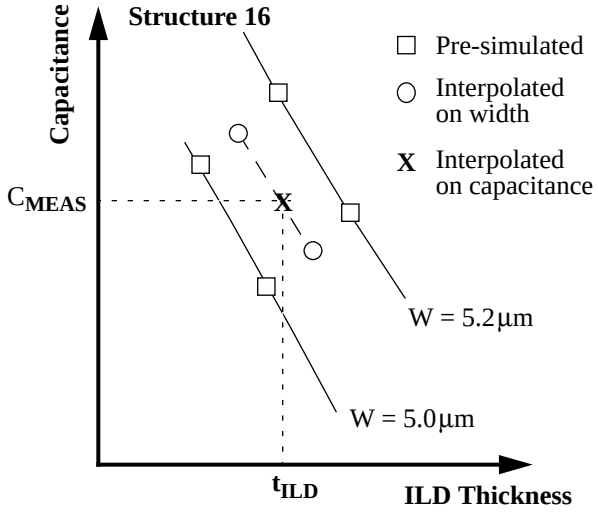


FIGURE 10. Two-dimensional interpolation for ILD thickness computation.



6. DATA ANALYSIS AND RESULTS

Measurements were taken from 52 die on each of 12 wafers (6 wafers each at 5000 Å and 6000 Å BPSG nominal deposition thickness). The goals of the data analysis in the first pass experiments are to identify the key factors giving rise to ILD thickness variation, and to estimate the magnitude of these contributions. Second pass experimental designs can then focus in on these factors, with the goal of building a predictive model of variation as a function of key parameters. Exploratory data analysis is shown in Fig. 11. This main effects plot indicates that the finger line width has the largest impact with appreciable effects from line spacing, finger lengths, and number of fingers. Histograms of ILD thickness for wafers B7 and D7, shown in Fig. 12, indicate a bimodal distribution. This is confirmed by cumulative normality plots, and more to the point, by scatter plots of the thickness values, shown in Fig. 12, which clearly indicate the impact of both die position within the wafer, and the main effect of the finger line width. The variation within each band in Fig. 12 is due to systematic variation resulting from the other factors and the remaining “random” variation. Analysis of variance (ANOVA) gives a breakdown of the variance

explained by each factor in the design. In this analysis, we also explicitly include the effect of the capacitor location within the wafer, and find that the die effect is almost entirely due to the spatial y coordinate. The resulting breakdown of the largest components from the ANOVA is pictured in Fig. 14.

FIGURE 11. Main effects from experimental design, wafers B7 and D7.

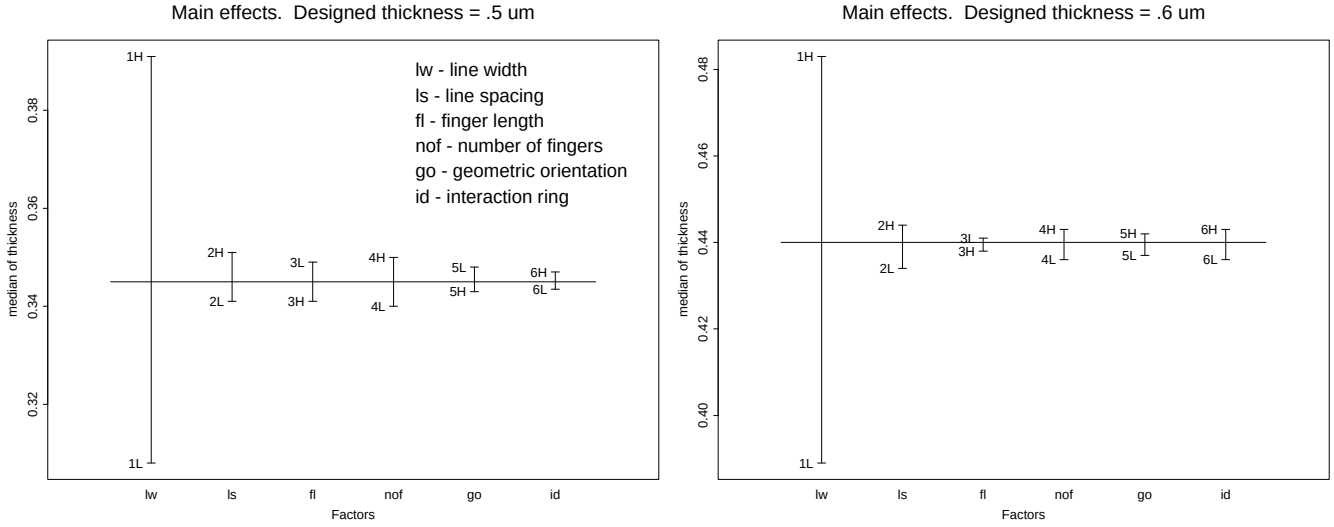


FIGURE 12. ILD thickness distributions, wafers B7 and D7.

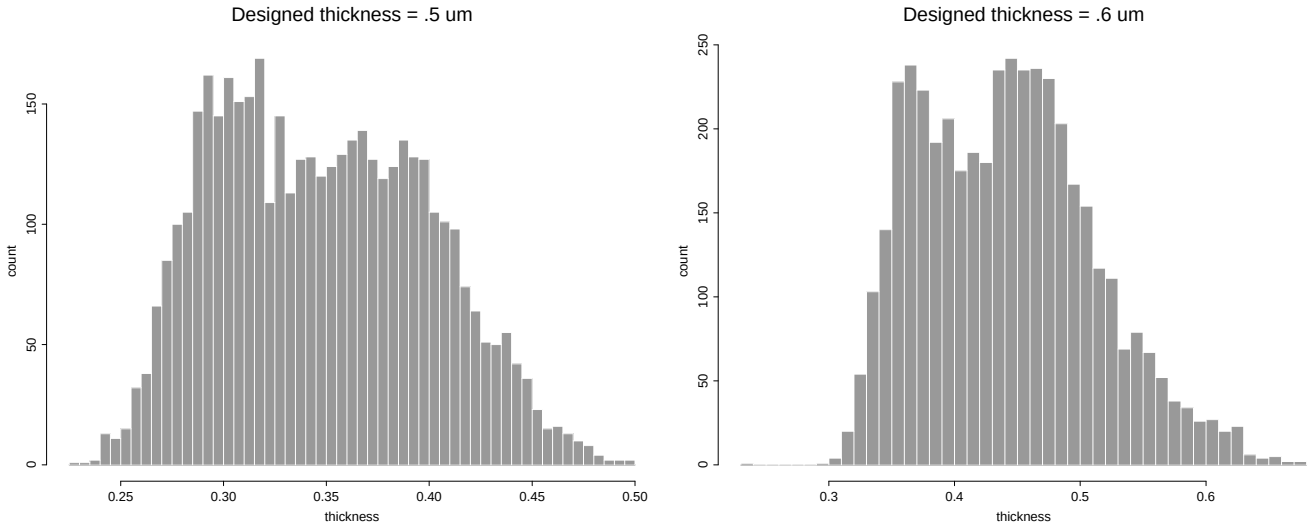


FIGURE 13. Scatter plot of ILD thickness, wafers B7 and D7.

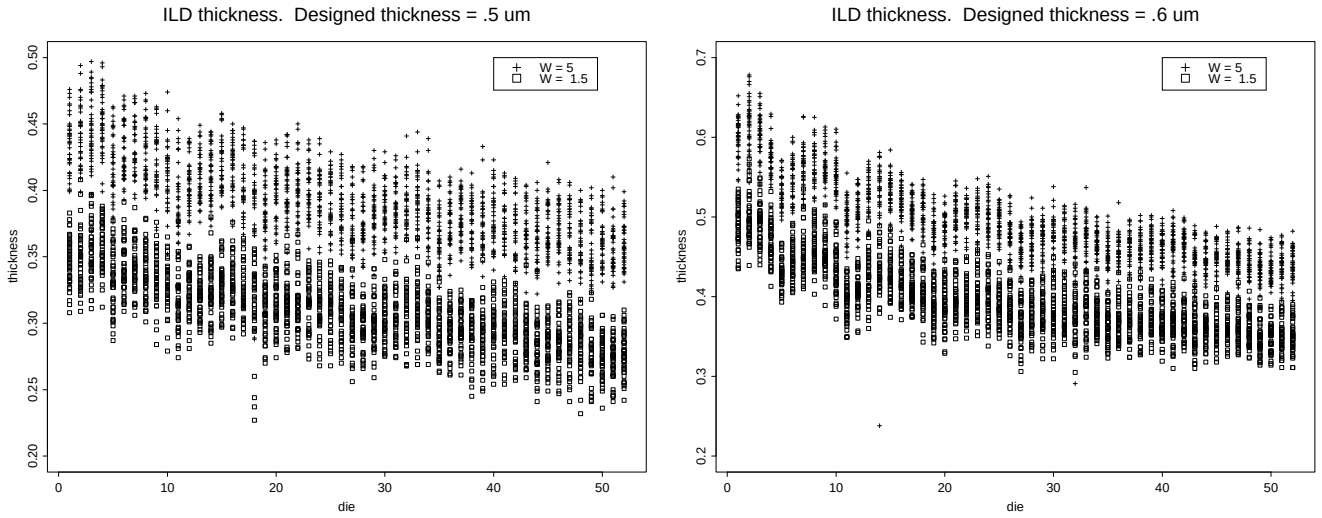
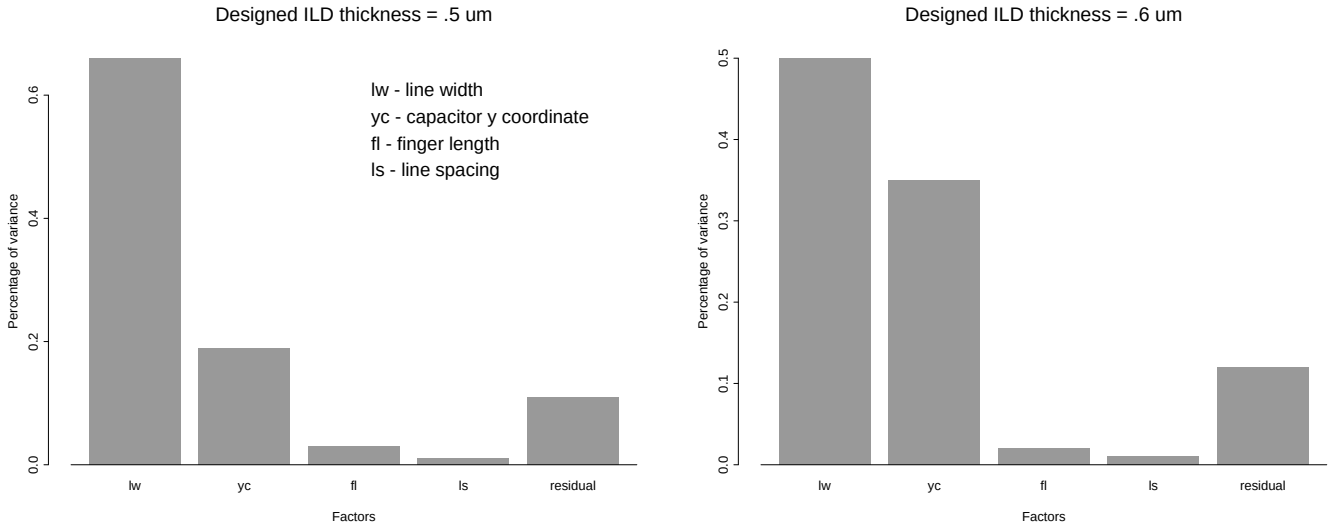


FIGURE 14. Contributions to variance by each factor, wafers B7 and D7.



7. CONCLUSIONS AND FUTURE WORK

The variation of ILD thickness is being studied using statistical metrology. First pass experimental designs have highlighted key factors affecting ILD thickness in a BPSG reflow planarization process. In future work, the statistical metrology methodology will be further exercised. Second pass experimentation at MIT is being pursued using the knowledge gained about important factors; the goal is to more finely quantify and model the relationships between factors and ILD thickness variation. Interactions with the metrology of line width variation will be studied. Application of additional statistical approaches, including filtering as suggested by Yu et al. for polysilicon critical dimension,[1] will also be examined.

Redesign and adaptation of the ILD statistical metrology approach for alternative planarization processes, specifically CMP, is also underway. In this case, it is believed that area/density concerns are more important than feature scale dependencies;[11] test structure modifications to assess this variation source are being developed.

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