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Wafer-Scale Modeling of Pattern Effect in Oxide Chemical Mechanical Polishing

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ABSTRACT

Dielectric film thickness variation arising from layout pattern dependency remains a major concern in oxide CMP. The severity of the pattern density effect is a function of the die location on the wafer, thus a combined wafer/die pattern dependent polishing model is required to fully assess the effectiveness of the process for a given planarization requirement. In this work, a two stage modeling methodology which accounts for both wafer-scale variation and within-die pattern dependencies, as well as their interaction, is developed. The effectiveness of the methodology is demonstrated over a range of polishing process conditions and consumable choices. We find that the integrated wafer/die CMP model accurately predicts the resulting increase or decrease in die-level pattern dependencies as a function of die position on the wafer.

Key words: pattern density, pattern effect, planarization length, chemical mechanical polishing, die-level variation, polishing pad, variation decomposition.

1. INTRODUCTION

Chemical mechanical polishing (CMP) has emerged as a critical process for global and local planarization in silicon integrated circuit (IC) fabrication.[1] In order to meet metal reliability and depth of focus constraints for submicron interconnect, extreme local planarity is required. Even more demanding are depth of focus requirements for global planarity across the entire stepper field which may be as large as 20mm x 20mm.[2] Compared to other planarization techniques, CMP achieves good global planarization in areas of constant pattern density. However, variation in pattern density across a die results in severe thickness variation at length-scales larger than the planarization length of the polish pad. In typical polishing processes, there also exists a systematic wafer-level variation in removal rate, which is a well known issue in process design and control. An important consequence of such wafer-level variation is that the pattern dependent variation of a die is thus also a function of the die location on the wafer. That is, the total range of variation within a die caused by pattern dependencies will also depend on which die on the wafer is examined. Effective modeling for pattern effects in CMP must account for the wafer-level variation as well as the local die pattern dependency, and must further account for the interaction or coupling between these two variation dependencies. With accurate integrated wafer/die models, process control and optimization can be improved; the improvements include identification of appropriate monitoring measurement points on the die and wafer, selection of process conditions and consumables which best achieve both wafer-level and die-level uniformity requirements, and integration with sensor-based control approaches to minimize process cost and environmental impact.

In previous work, we have described individual elements of a CMP variation modeling methodology.[3,4] In this paper, we further previous modeling work to contribute an integrated or combined wafer/die CMP model. Our previous work is illustrated in Figure 1, where the relationship of the new model to the previous work is also identified. In the first layer of Figure 1, the purpose of statistical decomposition is to identify and separate the contributions to oxide thickness (z) variation after polishing. Specifically, we create an additive statistical model of the form

$$z_{\mathrm{TOTAL}}(x, y) = z_{\mathrm{WLV}}(x, y) + z_{\mathrm{DLV}}(x, y) + z_{\mathrm{INTERACTION}}(x, y) + \varepsilon \tag{1}$$

where $z_{\mathrm{TOTAL}}(x, y)$ is the oxide thickness at some position x, y on the wafer, $z_{\mathrm{WLV}}(x, y)$ is the wafer-level variation, $z_{\mathrm{DLV}}(x, y)$ is the "die pattern" identical for every die, and $z_{\mathrm{INTERACTION}}(x, y)$ captures the interaction between the wafer-level and die-level variation. Statistical methods that take advantage of spatial characteristics of each type of variation (e.g. smoothly varying wafer level variation, periodicity of die across the wafer) are used to separate and construct spatial maps for each component from a given set of measurements. In the second level of Figure 1, more detailed modeling of specific varia-

tion components is accomplished. First, statistical regression models for wafer level variation can be constructed. More importantly, an analytical model explaining the effect of pattern density on the resulting oxide thickness has been developed.[8] In previous work, the interaction components have not been thoroughly studied or modeled. In this paper, we present a physically motivated model that inherently integrates these three components. An important result is that the model combines the wafer-level and die-level information in a nonlinear fashion to capture the total (deterministic) oxide thickness resulting from CMP. That is, we produce a two stage model of the form:

$$z_{\mathrm{TOTAL}}(x, y) = g(K_{\mathrm{WLV}}(x, y), L(x, y), W) \tag{2}$$

where g is the physical pattern-density analytic polish model, $K_{\mathrm{WLV}}(x, y)$ is a wafer-position dependent blanket polishing rate (which is itself dependent on the process), $L(x, y)$ is the die layout, and W is a density "window" function that parameterizes the planarization length or planarization response of the pad and process.

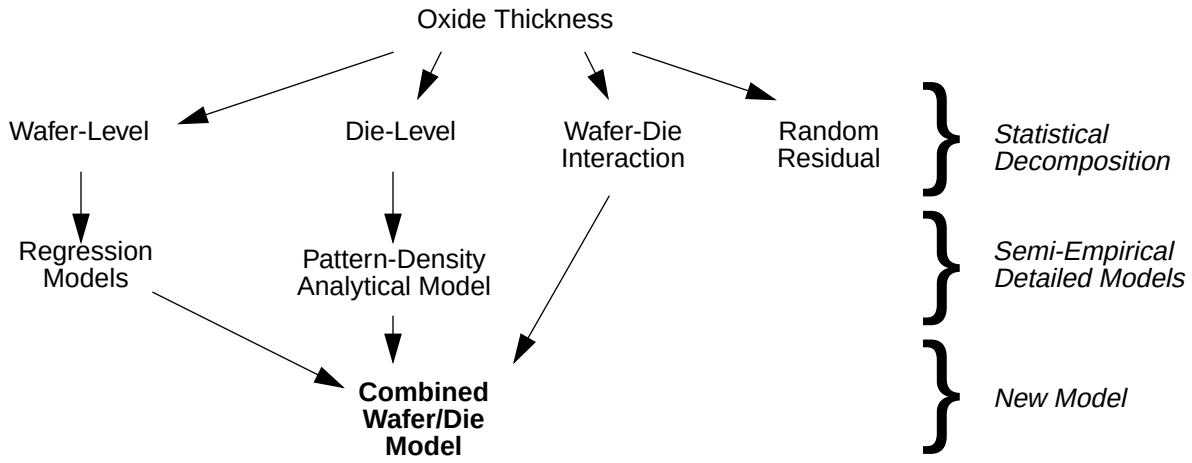

Figure 1. Previous work and new contribution to CMP variation modeling.

In Section 2, we briefly review other published work on CMP wafer-level and pattern dependent modeling. In Section 3, we introduce the polishing experiments and mask sets used here to develop and validate the new combined wafer/die CMP model. A variation decomposition (as in the first layer of Figure 1) is presented in Section 4 for these experiments, illustrating not only the wafer-level nonuniformity and the die-pattern dependence often observed, but also showing the importance of the wafer-die interaction in producing different oxide thicknesses for different die on a wafer. In Section 5, we describe in more detail the die-level pattern dependent polishing model, including suggestions for extraction of the density window function *W*. Similarly, Section 6 describes in more detail the wafer-level regression models (layer 2 in Figure 1) developed to capture the spatial dependence of the blanket removal rate $K_{\mathrm{WLV}}(x, y)$. These model components are then functionally combined in Section 7 to produce the new wafer/die CMP model. Model verification with experimental data for a range of polishing process conditions and consumables such as pad type is presented in Section 8 and conclusions are offered in Section 9.

2. BACKGROUND

Understanding and modeling of pattern dependent effects in CMP is crucial for successful use of the technology in mainstream dielectric planarization. Several modeling efforts have focused on local feature erosion or on die-level pattern dependencies. Other research has been reported on wafer scale modeling. We briefly summarize CMP models in these areas, as the background to detailed discussion of the CMP model proposed here.

Several models have been proposed to account for pattern effects in CMP[5,6,7] but their applicability has been limited. The limitations range from being based on non-representative test structures to probing of small process windows which limit the utility of the models beyond the scope of the original experimental conditions. A detailed review of the current state of CMP modeling has been provided by Nanz and Camilletti.[10] Most of the models, with the exception of those proposed by Hayashide et al.[9] and Stine et al.[8] do not apply across a whole die but rather focus on individual features. Other models have been pro-

posed, e.g. by Wang et al.,[13] to explain wafer scale or wafer level dependencies in polish rates. No model we are aware of has attempted to account for pattern dependent effects across the whole wafer.

While a variety of pattern dependent effects have been examined (such as size of individual features and spaces, pitch, amount of exposed feature edges), recent work has indicated that pattern density is the most important pattern factor in oxide CMP.[8] (This finding will be illustrated in Section 3 and 4.) The pattern density is defined as the ratio of the raised (or "up") area to the total area of a region on the chip or wafer. The total area within which density is defined is critical to accurate modeling, and is based on the planarization length of the polishing pad which depend on the process. Local pressure is inversely proportional to the pattern density, thus, from the Preston equation[12] the polish rate varies with pattern density across the die giving rise to post-polish oxide thickness nonuniformities.

3. PATTERN DEPENDENCY EXPERIMENTS

As a prelude to effective modeling of CMP for oxide planarization, polishing experiments were done for a wide range of die topography patterns. A set of four masks[14] shown in Figure 2 was used to generate the die patterns. Mask I explores the effects

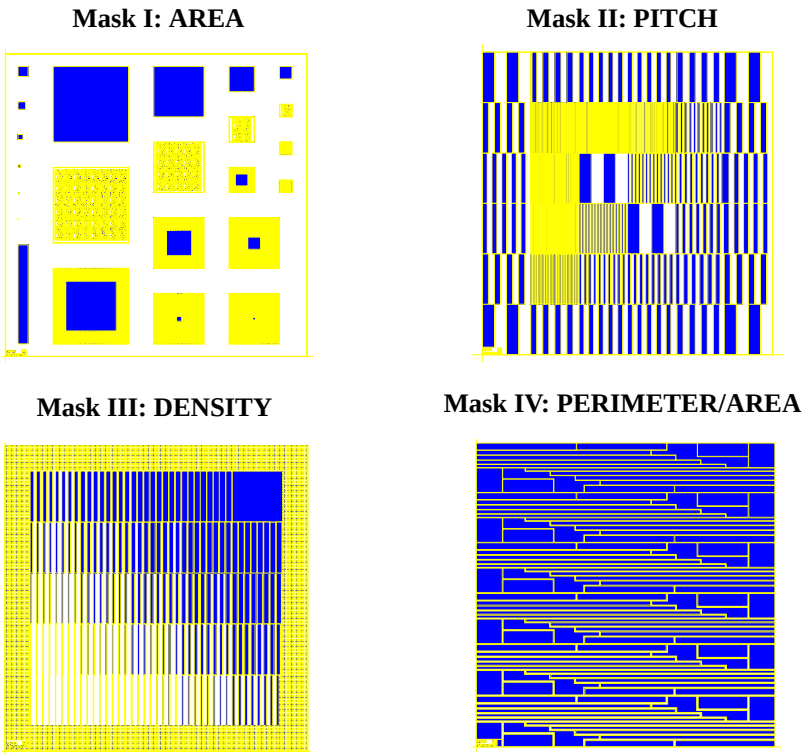

Figure 2. Characterization Mask Set.

of area and consists of blocks of sizes ranging from 20μm to 3000μm. It also contains blocks which mimic realistic circuit layouts. Mask II examines the effect of pitch. The pattern density – defined as the ratio of line width to pitch – is maintained at 50% while the pitch is varied from 2μm to 1000μm in the 2mm x 2mm blocks. Mask III explores the effect of density which is increased from 4% to 100% in steps of 4%. Pitch is maintained at 250μm in each of the 25 2mm x 2mm blocks. Mask IV explores the effects of block perimeter. It consists of blocks of constant area (1mm x 1mm) but with different perimeter/area ratios. The mask is divided into six sections and the spaces between the blocks are decreased from 60μm at the bottom to 10μm at the top.

These masks were used in a single-mask fabrication process to generate surface topographies on 6" wafers to be planarized using CMP. The fabrication process consisted of 1000nm LPCVD TEOS deposition, metal deposition, pattern and etch followed by 2000nm TEOS deposition. A typical final cross-section before CMP is shown in Figure 3 which also shows typical areas where optical measurements were taken.

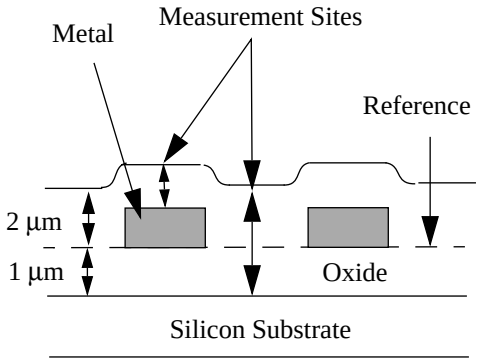

Figure 3. Cross-section before CMP.

Process (High, Low, & Center Setting)	Down Force (psi)	Table Speed (rpm)	Time (s)
A(L, L)	4.0	20	470
B(H, H)	8.0	50	112
C(L, H)	4.0	50	242
D(H, L)	8.0	20	228
E(C, C)	6.0	35	200

Table 1: Process Experiment Conditions.

Two sets of polishing experiments were done. In the first experiment all the masks were used, and down force and table speed, the two key factors affecting the removal rate, were varied as detailed in Table 1. Other polishing conditions held fixed were as follows: Rodel K-Grooved IC 1400 pad, Cabot SS 25 slurry, 20 rpm carrier speed, and 2 psi back pressure. Polishing was done on a Strasbaugh model 6DS-SP polisher with a dual head although only one head was used in this experiment. Wafers were also polished for 1/3 and 2/3 of the total polish time for each process to study planarization evolution with time. The final polish times were set to ensure an equal thickness removal (in the high density regions) for all the processes as the goal was to determine the effect of process on uniformity in addition to modeling the planarization evolution. In the second experiment, only the density mask (Mask III) was used. Two pads, IC 1000/Suba IV perforated and IC 1400 K-Grooved, were used and the down force was varied to examine its role in determining the planarization length which was the parameter of interest. The experiments were performed on an IPEC/Planar 472 polisher, the table speed was 32 rpm, carrier speed 28 rpm and other process conditions were similar to the experiments described above.

4. EXPERIMENTAL RESULTS - VARIATION COMPONENTS

Wafer-level polish characteristics are a strong function of the polishing process conditions and choice of consumables such as pad. Figure 4 shows the extracted wafer-level profile ($z_{\mathrm{WLV}}(x, y)$ in Equation 1) for polish data using Mask III. The extraction was done using a variation decomposition technique[3] and the raw data were measured over metal areas. As can be seen in the figure, different conditions of down force result in different degrees of wafer-scale non-uniformity. For the data presented, high radial wafer-level non-uniformity results for the high setting of down force and table speed.

For any process setting, the oxide thickness at various points within the die depends greatly on the pattern topography. Figure 5 shows the extracted die-level variation ($z_{\mathrm{DLV}}(x, y)$ in Equation 1) obtained using variation decomposition analysis of the raw data for process B (Table 1), for each of the four characterization masks. The extracted die-level variation is that contribution to variation that is exactly the same or held in common between every die on the wafer, and captures the contribution from the unique die layout. Note that only data over the raised (metal) areas is shown, as this is the primary oxide thickness of concern.

In Figure 5, we see that dies patterned using the area and density masks display the greatest variation due to layout pattern effect. This is consistent with the hypothesis that the pattern density is the key determinant of the polish rate for oxides. Note the weak effect of pitch despite the fact that the pitch values ranged from 1µm to 1000µm. The polishing characteristics of the varying pitch but constant density topographies demonstrate the effectiveness of CMP in achieving high global planarity in large regions of constant density. Furthermore this is achieved for relatively large feature structures. Data was not sampled with enough resolution to account for corner rounding of large features or blocks, which could be a concern if local planarity is not achieved. However, the results provide motivation for density based oxide thickness prediction for CMP.

To illustrate the interaction between wafer-level variation and die-level pattern dependency, we examine the total oxide thickness for sample die near the center and near the edge of the wafer for process B. As illustrated in Figure 6, we see that the die pattern is significantly different in the two cases: the range of variation in the center die is approximately 10% larger than the range in variation for the edge die. The wafer-level nonuniformity thus has a significant impact on the pattern dependent

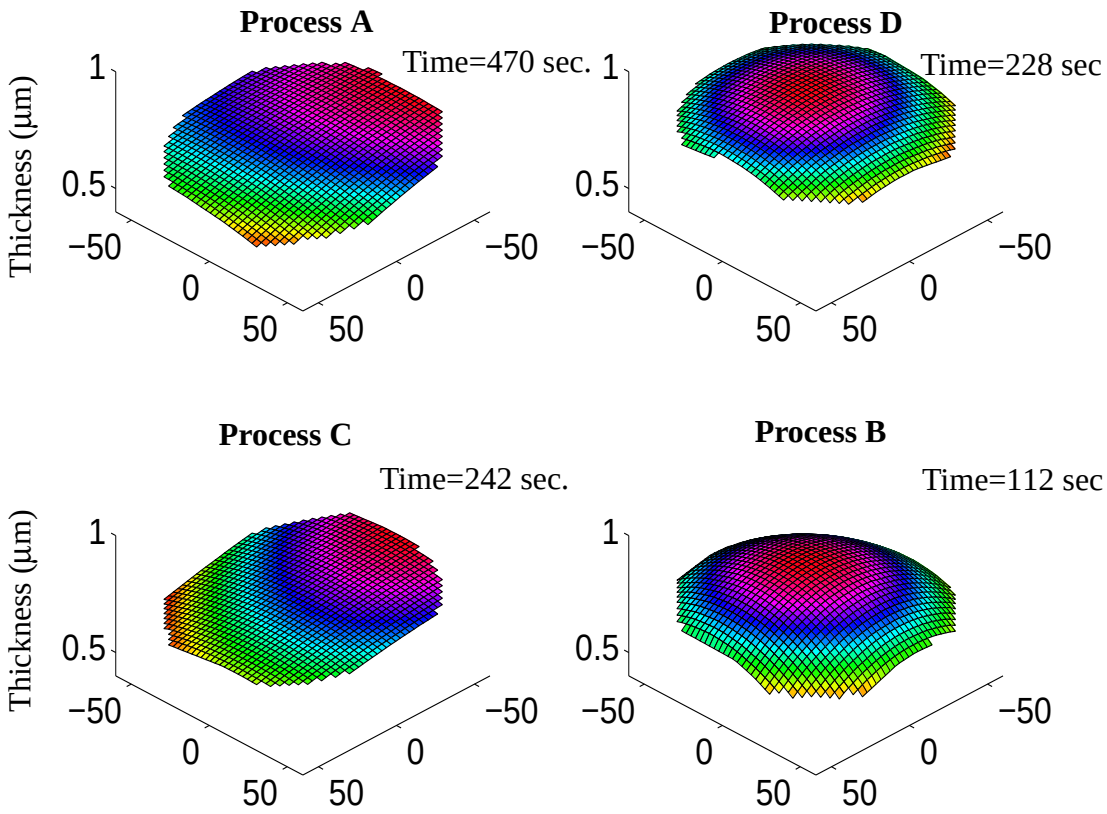

Figure 4. Wafer-level variation dependence on process conditions.

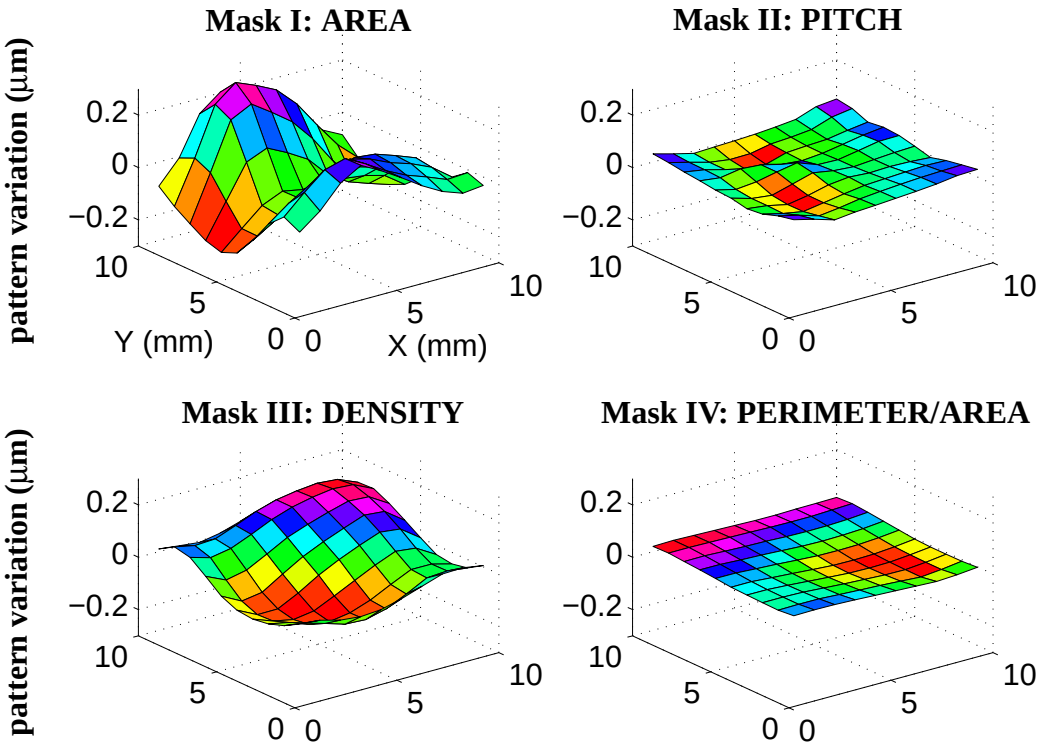

Figure 5. Die-level polish characteristics for the characterization masks.

polish characteristic depending on the location of the die on the wafer. The accurate prediction of such planarization at different locations is a key contribution of the new model detailed in Sections 5 through 7.

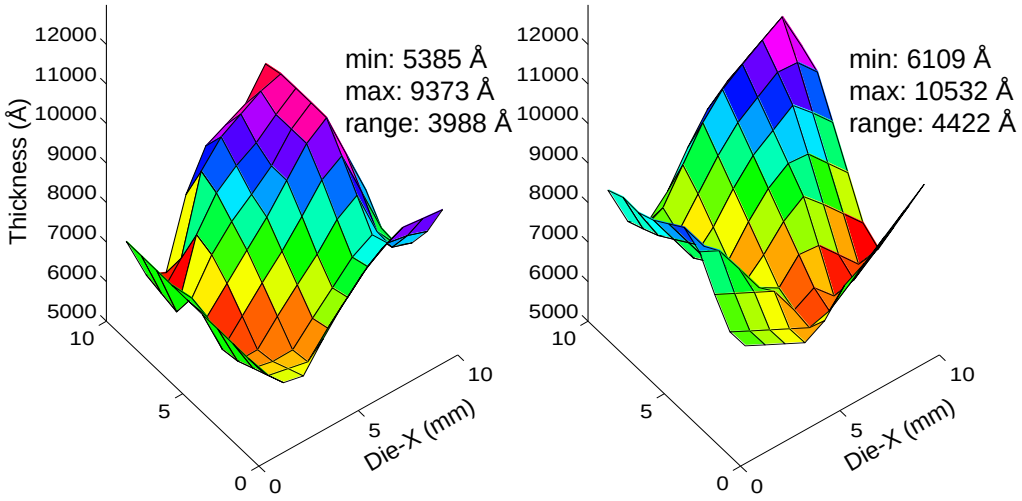

Figure 6. Oxide thicknesses for a die near the edge (left) and center (right) of the wafer.

5. LOCAL DENSITY BASED MODELING

In this section we focus on the detailed model for the fundamental pattern density polish dependency. In Section 6 we summarize the wafer-level modeling of polish rate, and then we combine these models for integrated wafer/die modeling in Section 7.

Model

Stine et al. proposed a CMP pattern dependent model that results in a closed form oxide thickness prediction.[8] The model is based on the Preston equation and gives the oxide thickness z as:

$$z = g(x, y, K) = \begin{cases} z = z_0 - \left(\dfrac{Kt}{\rho_0(x, y)}\right) & Kt < \rho_0 z_1 \\ z = z_0 - z_1 - Kt + \rho_0(x, y) z_1 & Kt > \rho_0 z_1 \end{cases} \tag{3}$$

$$\rho(x, y, z) = \begin{cases} \rho_0(x, y) & z > z_0 - z_1 \\ 1 & z < z_0 - z_1 \end{cases} \tag{4}$$

where K is the unpatterned wafer polish rate (assumed constant across the wafer) for the process under probe and $\rho_o(x, y)$ is the local pattern density. Other variables are defined in Figure 7. In this model, a key process/consumable dependent factor is the region over which density is defined for any point. In the original implementation,[8] density was defined within a square window centered at the point of interest; the density assigned to each point is the ratio of the total raised area to the total window area. Intuitively, the window size represents the length scale at which the pad returns to being relatively flat when perturbed by raised features. This is the planarization length or interaction distance for the pad. The effect of features that are greater than half the interaction distance away from the point of interest are ignored. A square window simplifies density evaluation but a circular window represents the expected circular symmetry of the pad more closely. A weighted window is also more appropriate since the structures closest to the point of interest have greater influence on the polish characteristics of a point. In a weighted window, the raised area contribution to the pattern density is a weighted function of the distance from the point of interest. Ways of determining the shape and weighting of the density window are developed later in this section.

In addition to the window properties, the raised area must be properly defined. Conformal depositions result in the most clearly and sharply defined raised areas. For other deposition profiles, use of a deposition profile simulator is recommended to

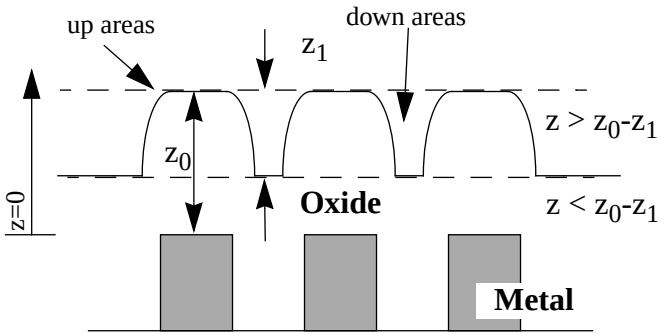

Figure 7. Definition of terms used in (3).

approximate the raised area as a function of feature height. For large features and conformal deposition, the raised area is approximated by the metal area which may be rapidly determined directly from the layout. Once polishing is underway, the raised area changes (e.g. for non-conformal deposition profiles). In the case of conformal deposition, constant density is assumed until local planarization is achieved and a density of unity (100%) is attained.

The model predicts the polish characteristics of the raised area only, and is appropriate for determining oxide thickness variation resulting from CMP. For typical oxide planarization processes where the local patterns are completely planarized, this limitation has no practical disadvantage. The model assumes negligible polishing of the down areas in determining the point at which density changes to 100%; extensions to overcome this limitation are possible. This approximation is valid for down features as large as 15% of the planarization length – this observation is based on polishing characteristics of the pitch mask which satisfied the model although the down features were as large as 500μm and planarization length of the pads was as small as 3mm. Modification is required if the down area polish rate is required as in polishing for shallow trench isolation (STI). Work is underway to develop such extensions. However, modeling the oxide polish phase in STI should fully benefit from the model.

Determination of Planarization Length

Accurate determination of the planarization length of the pad is key to effective local pattern dependent modeling. In this section we present three different but complementary ways of determining this value. The planarization length may be determined through regression, by direct measurement if a special mask is used to generate a step density topography, or through convolution and discrete filter design technique.

In the regression method, one assumes a certain window shape and then varies the window size to obtain the best model fit to data. In the case of a square window, for each window size considered the evaluated density using that window size is used to fit a model of the measured data; the window with the best model correlation is chosen. Note that for $Kt > \rho_0 z_1$, Equation 3 is linear in density with a coefficient of z_1. Planarization length determination using the regression method[8] reduces to accurate measurement of z_1 and modeling of final thickness as a function of density such that the gradient of the slope is z_1. This method succeeds if polish time is long enough such that local planarization is achieved. Figure 8a shows a typical plot of the model correlation as a function of the polish length with the window assumed to be square. The regression method is useful for topographies with gradual density variation such as those obtained using Mask III. The results may then be applied to arbitrary layout to predict within-die thickness variation.

In the direct planarization length determination, a special layout mask is used to generate step densities as shown in Figure 8b. The planarization length is then measured via a series of measurements of thickness along the step density change. In this method, regions of constant density must be longer than the expected planarization length. A trace of the thickness after CMP as shown in Figure 8b may thus be considered to be the step response of the given step density. Signal processing approaches in conjunction with assumptions about the two-dimensional window shape can then be used to extract the planarization length.[16] For example, Figure 9 shows the step response for a two-dimensional radially symmetric window filter with Gaussian weighting; in this case, the planarization length can be easily extracted as the second moment (standard deviation) or width of the Gaussian filter.

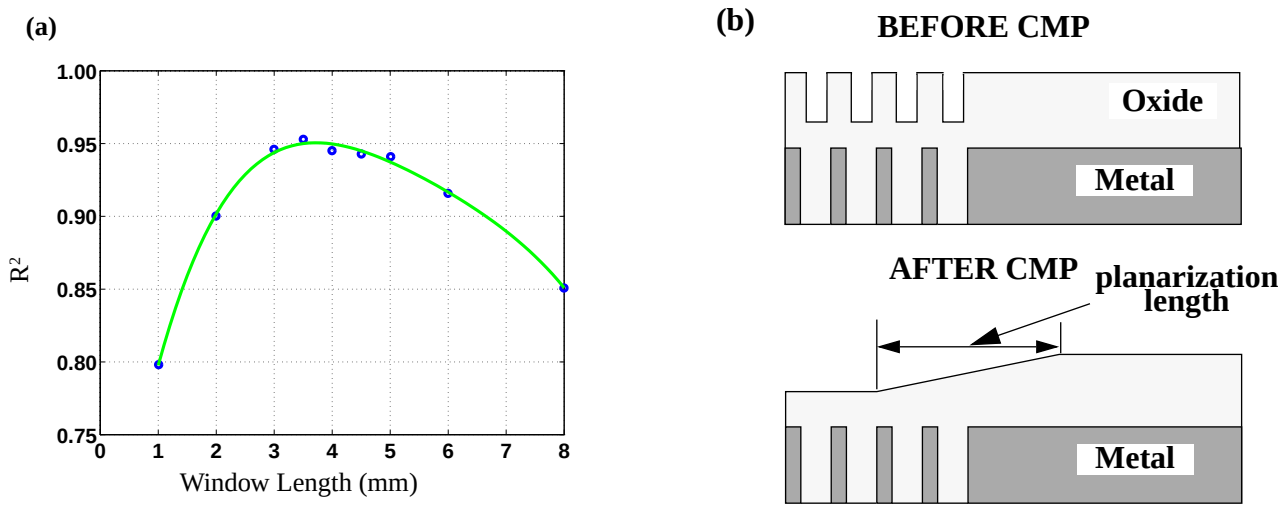

Figure 8. Model correlation vs. window length (a) and experimental determination of planarization length (b).

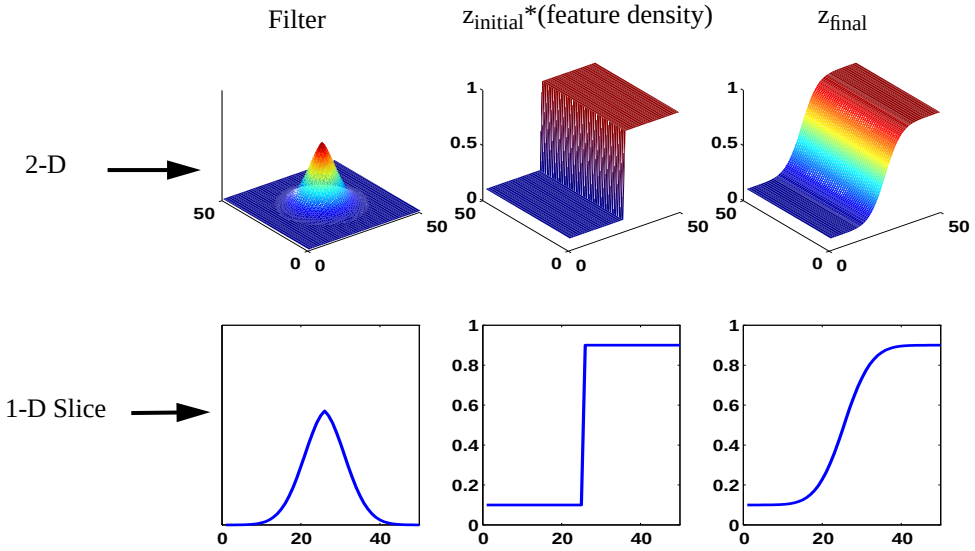

Figure 9. 2-D Gaussian window filter and step response.

In the third approach, the discrete filter analogy is taken one step further and full two-dimensional layout patterns (as opposed to the quasi-2D step function above) are used. If the chip is polished such that local planarity is achieved, the final thickness can be related to the initial thickness by the following expression:

$$z_{\text{final}}(x, y) = [z_{\text{initial}}(x, y) \cdot L(x, y)] \otimes W \tag{5}$$

where $\otimes$ indicates convolution and W is the density window filter. The layout feature density $L(x, y)$ is evaluated over a region much smaller than the planarization length, and in the limit is an indicator function (1 or 0) indicating if a pattern feature is present or not at a specific location. The appropriate two-dimensional filter W may be obtained iteratively with assumptions on radial window symmetry using discrete filter design concepts as detailed in numerous texts such as [15]. In this approach both the window shape and size may be obtained from initial and final surface topography data, if the test pattern is rich (or complicated) enough to provide sufficient data.

In this paper, the first method is used to extract planarization using regression to polish data. Experimental validation of the signal processing approaches is underway and will be reported in the future.

6. WAFER-LEVEL MODELING

In the previous section a model that accounts for local pattern density was presented. In this section, we summarize the model we use to capture wafer level spatial dependencies in the removal rate. By "wafer-level" we mean that component of variation that does not depend on the layout pattern. In particular, if a blanket (unpatterned) wafer is polished, the surface exhibits non-uniformity which is often radial. This is due to many factors including relative velocity mismatch across the entire wafer surface, non-uniform force distribution by the carrier, and non-uniform slurry flow between the wafer and pad.

Unlike modeling of the pattern effect, spatial modeling of wafer-scale removal rate is easily accomplished empirically since relatively few factors can account for a majority of the variation. An adequate model may be obtained using only down force, table speed, carrier speed and back pressure. To reduce effects of measurement noise, the removal rate should be determined at a minimum of 121 sites on a blanket wafer to fit a spatial model. For most polishing conditions, a second order model of the removal rate is adequate as given by:

$$R(x, y) = a + bx + cy + dxy + ex^2 + fy^2 \tag{6}$$

where a, b, c, d, e and f are model coefficients and x and y are spatial coordinates of the wafer. Conventional multiple regression approaches are used to determine significant coefficients in the above model. In addition, functional forms are possible[17] that capture the dependency of each coefficient in the above model on process conditions (e.g. to model a, b, c, etc. as a function of process conditions P such as down force, table speed, carrier speed, and back pressure):

$$R(x, y, P) = a(P) + b(P)x + c(P)y + d(P)xy + e(P)x^2 + f(P)y^2 . \tag{7}$$

7. COMBINED WAFER/DIE MODEL

In Section 4, we presented a decomposition of oxide CMP thickness data into orthogonal wafer-level and die-level components. Section 5 discussed in detail the pattern dependent component of the model, which depends on the die layout and planarization length for the calculation of ρ_0, which can be combined in a simple nonlinear function of polish time and local polish rate K to predict oxide thickness. In the previous section, we discussed the wafer-level modeling of the polish rate. In order to combine the component models in an appropriate fashion, all that remains is to relate R in Equation 7 to K in Equation 3. That is to say, we can use any good model of wafer-level polish rate (such as the empirical models in Section 6) to provide the appropriate polish rate constant K for each and every die on the wafer, which is then used to solve for the oxide thickness as a function of time and position on the die. Since wafer-scale variation is small within a die, it is sufficient to determine an average or effective K for each die i:

$$K_i = \frac{1}{A_i}\iint R(x, y)dxdy \tag{8}$$

where A_i is the area of each die and the limits of the integration are the opposite corner coordinates of the die. Given K_i and the window size and shape W (which determines the local density ρ_0), the oxide thickness can be computed using Equation 3 for any position on each die on the wafer.

As described above, K and W can be found for any given process; the combined wafer/die CMP model then provides a simple but effective way of determining pattern effects for arbitrary layouts and may be used to simulate the polishing characteristics of many different chips for the characterized process.

It is also possible to calculate the process parameter dependence of the combined wafer/die variation. The combined model requires two key characterization steps for such use: determination of the process parameter functional dependence in the wafer level model of Equation 7, and determination of the process dependence in the planarization length or window size W. Once these have been characterized for the process parameter space of interest, it is then possible to compare and evaluate the combined wafer/die trade-offs across many different layouts and process conditions. Note also that polish effectiveness of a pad is a function of the age of the pad and the conditioning techniques employed. One simple approach to evaluate the impact of pad wear on planarization performance is to update the wafer-level uniformity model for K based on monitoring measure-

ments, and then utilize the model to examine the resulting die nonuniformities at various locations across the wafer.

8. INTEGRATED WAFER/DIE MODEL RESULTS

In Sections 5 through 7, the combined wafer/die CMP model has been presented. In this section we demonstrate the effectiveness of this modeling strategy using data from the experiments detailed in Section 3. Only Mask III data is presented since similar conclusions may be drawn based on the results from the other three masks. Mask III has the advantage that it demonstrates the effect of density directly.

Process	Center Die K (nm/min)	Edge Die *K* (nm/min)	Polish Length (mm)
A	79.6	83.8	3.08
B	390.3	446.3	2.73
C	205.3	210.2	3.30
D	201.3	221.3	2.75
E	225.5	250.8	2.78

Table 2: Blank rate and planarization length.

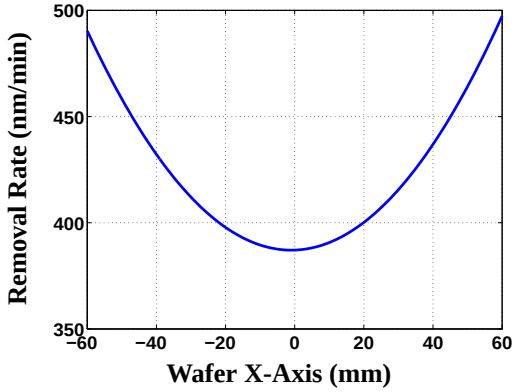

Figure 10. Radial dependence of *K* for process B.

Process Experiments

In the process experiment, down force and table speed were varied as detailed in Table 1. These factors affect both the planarization length of the pad and the effective blanket polish rate *K* for each die. Table 2 summarizes the effective *K* for an edge and center die as well as the planarization length for the processes. A diameter scan of the removal rate for process B obtained using Equation 6 is shown in Figure 10. This process had the worst wafer-level uniformity and it will be used to demonstrate the effectiveness of the methodology even in an extreme case. An examination of the table shows that the planarization length of the pad has a strong dependence on the down force and only weak dependence on table speed. The model fit for an edge and center die for process B is shown in Figure 11 and an excellent fit is apparent.

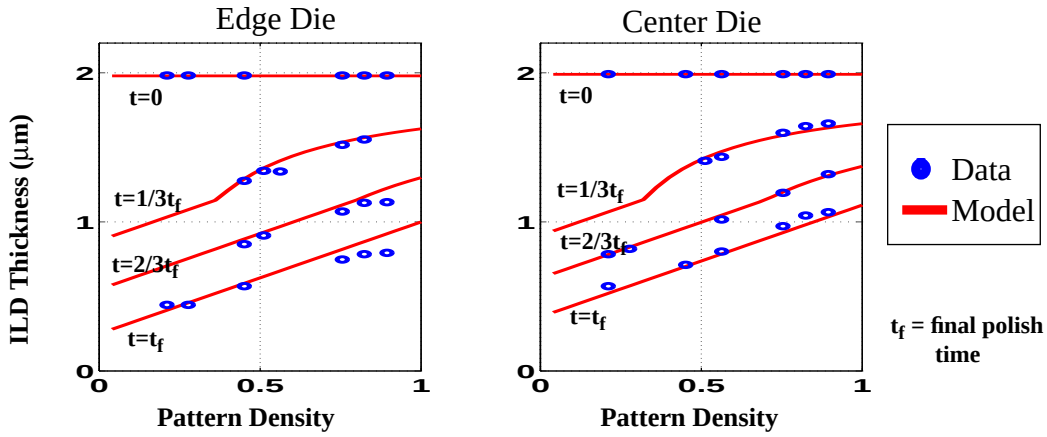

Figure 11. Model fit for process B.

Pad experiments

The pad type and down force also affect both the spatially dependent polish rate *K* and the planarization length. Figure 12 shows the diameter scan of *K* for the two pads under the two conditions of down force. The polish amount at 6 psi was less than at 8 psi and a shift in the 6 psi curve is required for magnitude comparison. However, high down force results in higher wafer level variation as the edge polishes faster than the center. Table 3 shows the planarization length dependence on force. High down force is indicated to have a longer planarization length which is a contradiction from the results of the process

experiment. The anomaly arose because the polish time at 6 psi was such that complete local planarization was not achieved across the entire wafer thus some parts of the wafer were still in the nonlinear regime of Equation 3. This underscores the importance of ensuring complete local planarization across the wafer in the determination of the planarization length. The model fit for 8 psi is shown in Figure 13 for the center and edge die for both pads. Excellent model fit is again apparent.

PAD	8 psi	6 psi
IC 1000/Suba IV	3.00 mm	2.72 mm
IC 1400	2.80 mm	2.66 mm

Table 3: Polish length dependence on pressure.

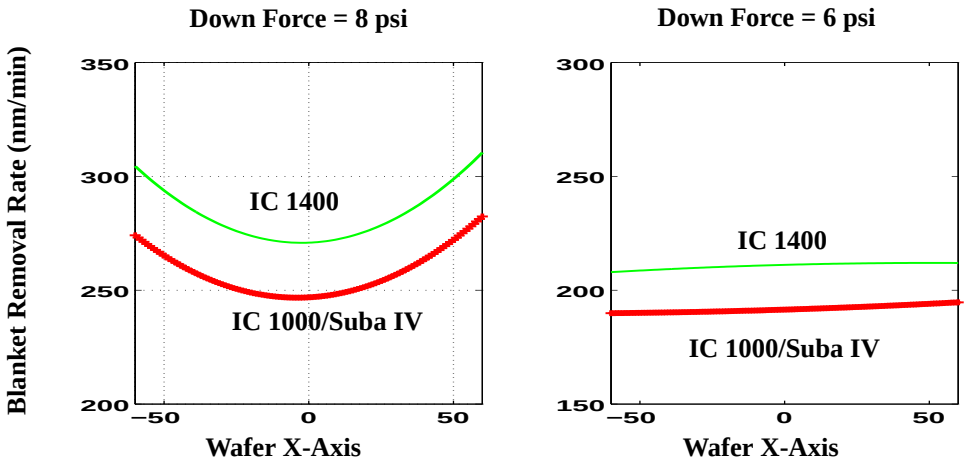

Figure 12. Radial dependence of *K* for the pad experiment.

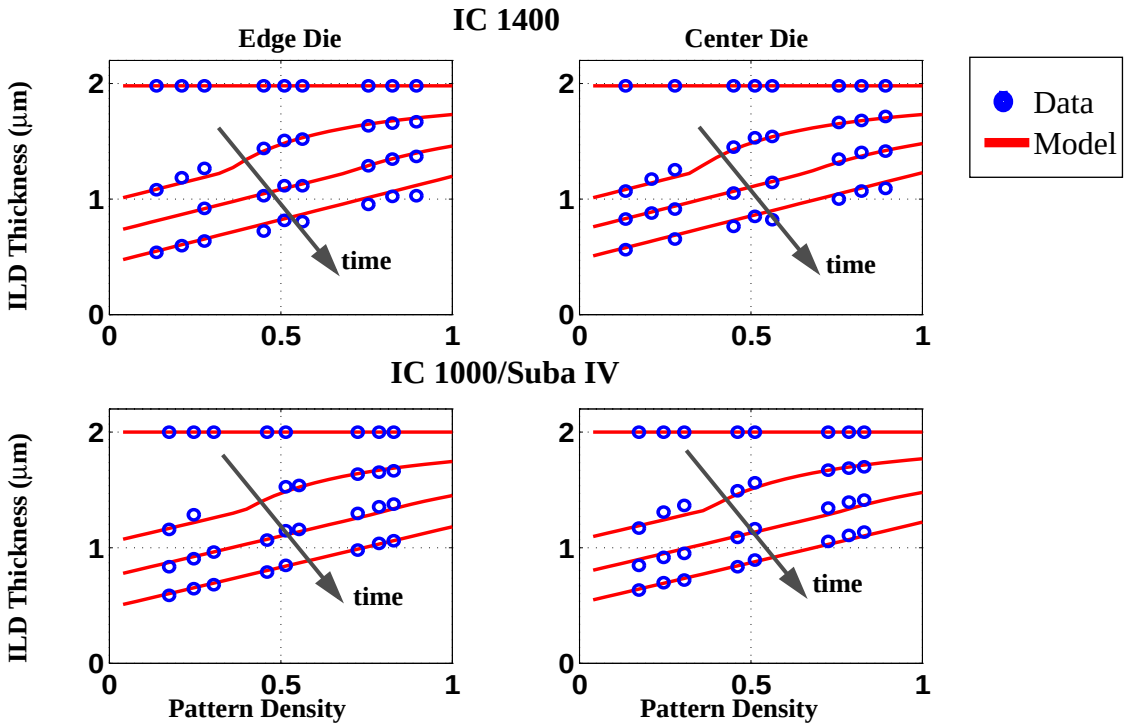

Figure 13. Model fit for different pads.

9. CONCLUSION

In this paper an integrated model that accounts for local pattern effects as well as wafer-scale variation in oxide CMP has been developed. It has been shown that by separately accounting for the local effects through a density model and incorporating wafer-scale polish rate variation, pattern-dependent effects may be determined for arbitrary pattern topography. The integrated model explains the resulting increase/decrease in the die-level pattern dependencies as a function of die position on the wafer and opens opportunities for process control and optimization incorporating pattern dependency in CMP.

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