PLANARIZATION AND INTEGRATION OF SHALLOW TRENCH ISOLATION

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ABSTRACT

STI process flow and planarization requirements are reviewed. An STI planarization mask was designed and utilized for test wafer patterning to investigate STI CMP planarization. Test wafers were processed through a typical STI process sequence, including trench etch, trench liner oxidation, trench-fill, and CMP. Two different CVD techniques, ozone TEOS thermal CVD and HDPCVD, were investigated for trench-fill. CMP experiments were carried out with different process parameters and consumables. Extensive CMP characterization was carried out utilizing multiple metrology techniques. The results fit the previously reported "CMP dielectric planarization" model [1, 2] quite well.

INTRODUCTION

Shallow trench isolation (STI) is an enabling technology for the fabrication of advanced sub-0.25 micron integrated devices. A typical STI process sequence includes the following process steps: pad oxide oxidation, LPCVD nitride deposition, trench lithography, trench etch, resist strip/clean, liner oxidation, CVD oxide trench fill, planarization, post-CMP clean/light BHF dip, nitride strip, pad oxide strip, sacrificial oxide oxidation, sacrificial oxide strip, gate-oxide oxidation, and gate deposition. Obviously, this sequence describes STI related processes only and leaves out many other front-end processing steps.

Requirements for STI planarization are much more stringent than those for inter-layer dielectric (ILD) planarization. Chemical mechanical polishing (CMP) has been accepted in recent years as a critical step in mainstream IC fabrication technology, and has enabled the fabrication of multi-level interconnect up to 5 or 6 metal levels. However, for STI planarization, CMP is "essential," but typically insufficient by itself in meeting all the requirements. Either or both of the following two different methods are commonly adopted to "assist" STI CMP: (1) imposing a design rule constraint for device layout to simplify the CMP, (2) adding a "reverse-mask patterned etchback" process prior to CMP [3]. Variations of these approaches also have been reported [4]. All these demonstrate the challenge of STI planarization.

STI PLANARIZATION REQUIREMENTS

Two of the essential requirements for STI planarization are: first, all the deposited trench-fill CVD oxide in the active regions (where oxide is over nitride) must be removed. Second, no erosion through the silicon nitride over active silicon regions should occur anywhere on the wafer. For better device characteristics and yield, there are two additional requirements: isolation oxide (oxide in trench regions) surface adjacent to active devices should remain above the active silicon surface, and the wafer surface should be nearly planar across all borders between active and isolation regions prior to poly-gate deposition. A lower isolation oxide surface is highly undesirable because it results in gate-wrap-around the silicon device corner which affects device threshold voltage and results in higher sub-threshold current [5].

Silicon nitride is the commonly used STI CMP stop layer with a typical thickness of 170 nm. This thickness may be reduced if CMP aids are used. For a theoretically perfect CMP process, the isolation oxide surface would be as much as 170 nm above active silicon surface (neglecting the pad oxide thickness). In practice many factors contribute to the lowering of the isolation oxide surface. To maintain the isolation oxide surface height at the same level as silicon surface or slightly above, the total allowable budget of oxide surface lowering for all factors combined is the initial nitride thickness. Figure 1(a) illustrates an abbreviated STI process sequence and Figure 1(b) shows the primary factors which contributes to the lowering of oxide surface.

These factors are further described in Table I, with the estimated contribution to oxide surface lowering listed. As shown in the Table, the total consumption of this planarization budget may exceed the available budget. The specific CMP process is then not "capable" of planarizing the STI structure since there may be

oxide residue over some active regions or the trench oxide surface may be below active silicon surface. In these cases, other techniques would be adopted or added as aids to CMP. This investigation focuses primarily on STI CMP. No reverse-mask etchback or other CMP aids are used. The objectives are to optimize the CMP process and to develop a set of device layout rules which would enable a CMP-only STI planarization process.

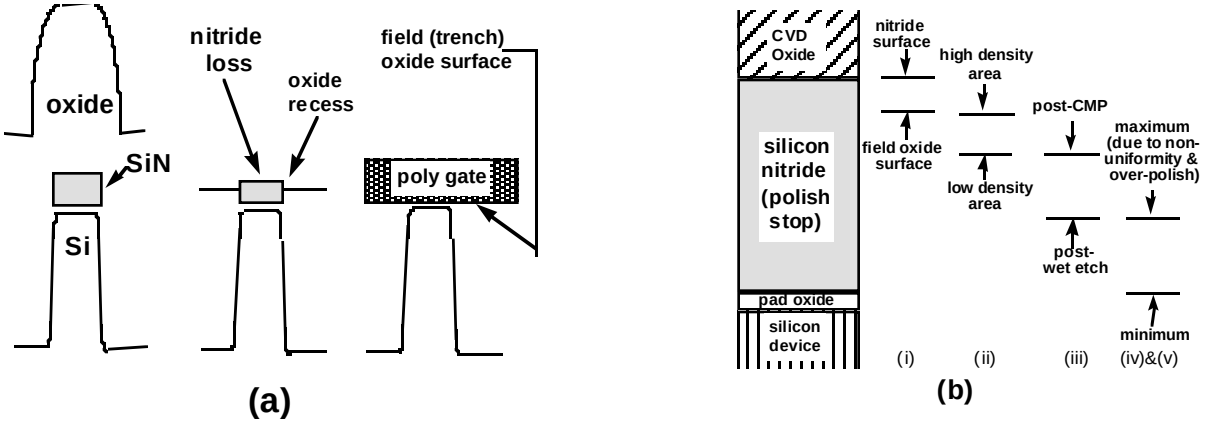

Figure 1. (a) Schematics of three intermediate STI structures: post-trench fill, post-CMP, and post-gate deposition; (b) key factors which consume available STI CMP budget

Table I. Key factors which contribute to the consumption of available process window

	Factors which lower isolation oxide surface	Estimated lowering (nm)	Description of the factor, source of data, and comments
i	Oxide recess (relative to nitride surface)	26	Isolation oxide surface is lower than adjacent nitride surface due to CMP selectivity, which is in addition to dishing of large width trench caused by pad bending. Data from AFM measurement.
ii	Pattern effect (device layout effect)	32 ++	Pattern density, feature size, nitride corner erosion, etc. Pattern density variation of 40% to 60% would by itself account for nitride thickness variation of 32 nm, see Fig. 4(a). Wider density range and other factors could greatly increase nitride thickness variation.
iii	Post-CMP Wet-etch	50	Three post-CMP wet-etch steps are typically required for device fabrication: 1) post-CMP HF dip to remove surface contamination, 2) strip of pad oxide, and 3) strip of sacrificial oxide
iv	Baseline nitride removal during CMP	20	This is required as part of manufacturing tolerance. This nitride loss can be reduced or eliminated with a well-controlled CMP process and a robust endpoint.
v	Non-uniformity of trench-etch, fill, CMP, and others	42 +	Estimation based on the following best-known-method results: ■ trench etch depth: max-min +/- 4% ■ CVD trench fill thickness: max-min +/- 3% ■ CMP polish rate: max-min +/- 8%
		> 170	**total isolation oxide surface lowering or variation**

EXPERIMENTAL RESULTS AND DISCUSSION

As reported previously [1, 2], dielectric CMP is pattern density dependent. CMP will polish the raised areas much faster than the lower areas until the surface approaches planarity. The effective pattern density at initial stages of STI CMP is the CVD oxide pattern density, instead of the mask density. The effective density at a spatial location is obtained using an elliptic weighting function which accounts for the neighboring topography [2]. This oxide pattern density depends on the deposition profile of the specific CVD technique. For advanced STI trench-fill, only two CVD techniques can provide the void-free trench-fill

capability: (1) silane based high density plasma (HDP) CVD, and (2) ozone-TEOS based thermal CVD in either atmospheric or sub-atmospheric (SA) pressure region. Figure 2 illustrates the deposition profiles of these two CVD techniques. While SACVD oxide profile is conformal, HDPCVD oxide profile is more complicated. Due to simultaneous deposition and sputtering removal, HDP deposition results in the characteristic 45° sidewall angle, and is self-planarizing where oxide is deposited over arrays of fine-pitch line and space structures. For those regions in a die with mostly large features (feature dimension is much larger than the oxide film thickness), the oxide pattern density is approximately equal to mask density. However, for regions with small features, the oxide pattern density can be dramatically different from the mask density. For example, an array of equal line and space with sub-0.5 μm dimension would have a mask density of 50%. However, the oxide pattern density will be close to 100% with SACVD filled STI and close to 0% with HDPCVD filled STI, as shown in Figure 2. Therefore, one should expect very different results between these two CVD techniques.

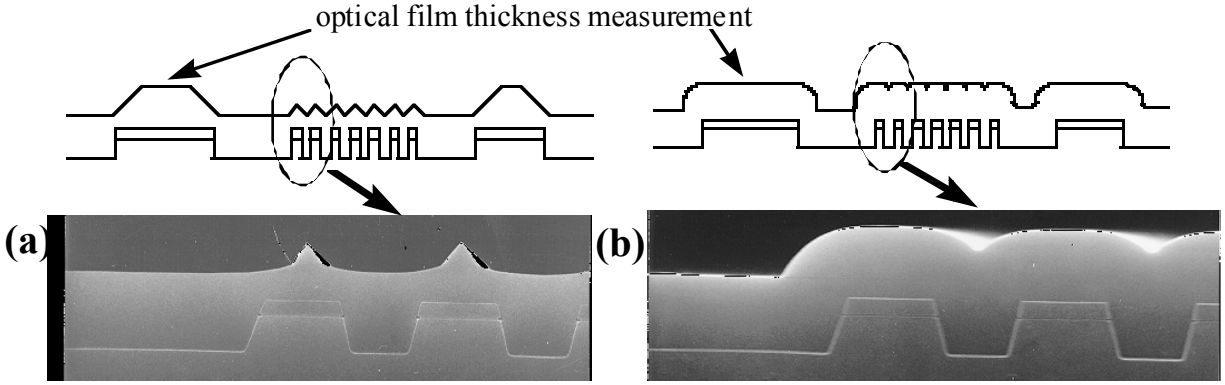

Figure 2. Oxide deposition profile over 1 μm line/space structure, (a) HDPCVD, (b) Giga-fill SACVD

The STI mask used for this investigation is shown in Figure 3(a). Each die is 20 by 20 mm in size, and consists of regions with different density or special structures. An elliptic weighting filter is used for the CMP modeling. The characteristic length is calculated to be 5.3 mm for a specific set of CMP parameters. Using this length, oxide pattern density is calculated for HDP and SA STI. Results are illustrated in Figure 3(c). Dramatic difference in oxide pattern density can be seen in the middle regions where many small dimension line and space structures exist. The effective density is not equal to the 50% local layout densities (i.e. equal line and space structures on the layout) along this line because the pattern density is averaged through the specific weighting filter. Toward either end of this 20 mm line, the oxide pattern density is similar between HDP and SA, and both are similar to the effective mask density because the structure dimension near the cut line ends is much greater than the oxide thickness.

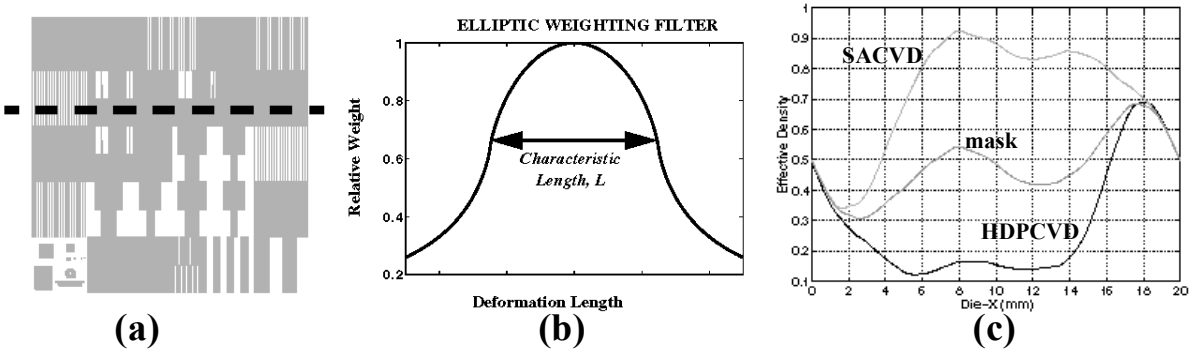

Figure 3. (a) STI CMP test mask, (b) elliptic weighting filter for effective pattern density calculation, (c) pattern density across the marked line in (a) for the mask and for SACVD and HDPCVD oxide

Optical film thickness measurement can be used to measure the polish rate. Due to the finite beam spot size, this technique can only be used where feature size is 10 μm or greater. Figure 4 shows two sets of baseline CMP results measured with this method. CMP was carried out using IC1000 pad and standard oxide slurry with approx. 4 to 1 oxide to nitride selectivity. The pattern density effect is shown in Figure 4 (a);

slower polish rate in regions with higher pattern density resulted in oxide residue over nitride or higher remaining nitride thickness compared to regions with lower pattern density. Figure 4 (b) shows the feature size effect where the individual active features are somewhat isolated. Lower local pattern density for smaller feature resulted in higher polish rate, and therefore, lower remaining nitride thickness. For this set of data, the measurement was done by stepping the beam at small increment along the center line across the active features until the figure of merit for the measurement deteriorated indicating that the beam was approaching the active/trench border. Even without accurate thickness measurement at the border, it is apparent that corner nitride at active edges polishes much faster than the interior of active regions, more than that accounted for by pattern density. This is believed to be caused by the higher local pressure once the trench starts to dish below the adjacent nitride surface.

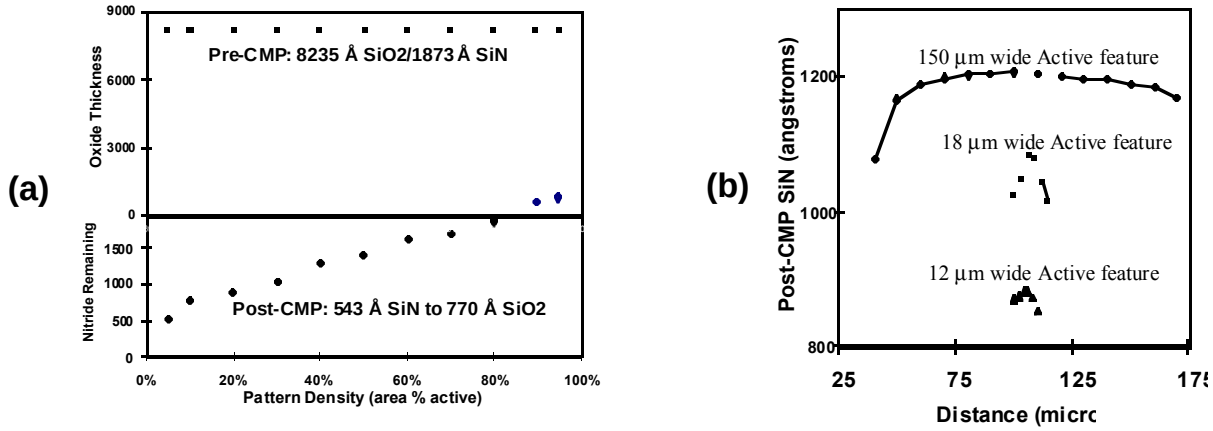

Figure 4. Post-CMP nitride thickness as function of (a) pattern density, (b) active feature size

A set of test wafers were polished at 50 second increments and the stacked film was measured optically at different pattern density regions after each polish step. As shown in Figures 5 and 6, the results fit the dielectric CMP model [2] quite well using the oxide pattern density taking into account the oxide deposition profile.

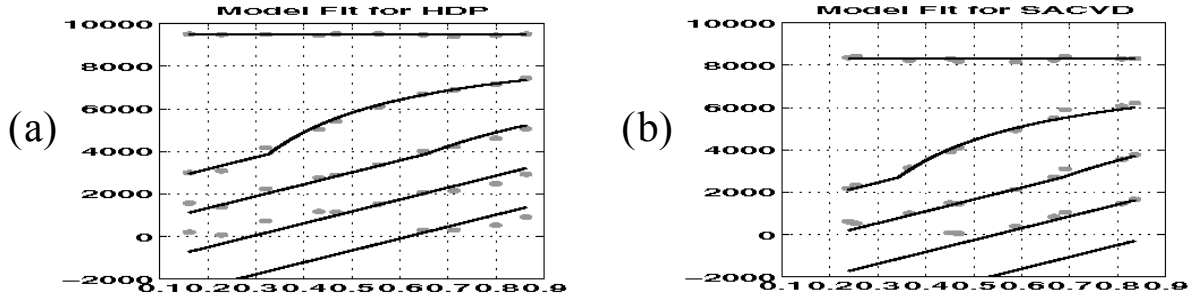

Figure 5. (a) Model fit for HDP filled STI in oxide phase; (b) model fit for SA filled STI in oxide phase

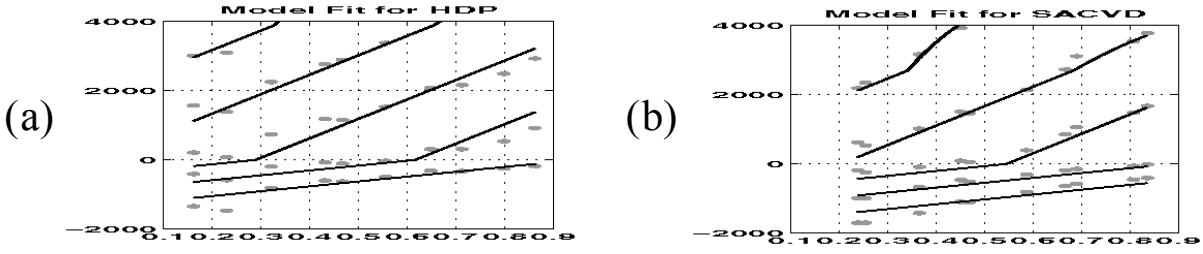

Figure 6. (a) Model fit for HDP filled STI in nitride phase; (b) model fit for SA filled STI in nitride phase

As shown in Figure 4 (b), nitride at active edge suffers additional thickness loss beyond that accounted for by pattern density. This phenomenon is further studied using SEM micrographs. Figure 7 shows the results of multiple SEM film thickness measurement across a 1 mm wide trench and a 1 mm wide active region. The trench oxide thickness is plotted on the left and the nitride thickness plotted on the right. The three

corresponding SEM's show sample cross-sections taken at the trench-active border, 100 μm to the left in trench region, and 100 μm to the right in the active region. It is clear that severe nitride thickness loss could occur at edge of active region, and the adjacent oxide surface would be further recessed from the surface of the thinnest nitride at the edge. This is one of the most serious threats to maintain the isolation oxide surface height. For data shown in this Figure, the sample was polished with high (nitride to oxide) selectivity slurry with large amount of over-polish.

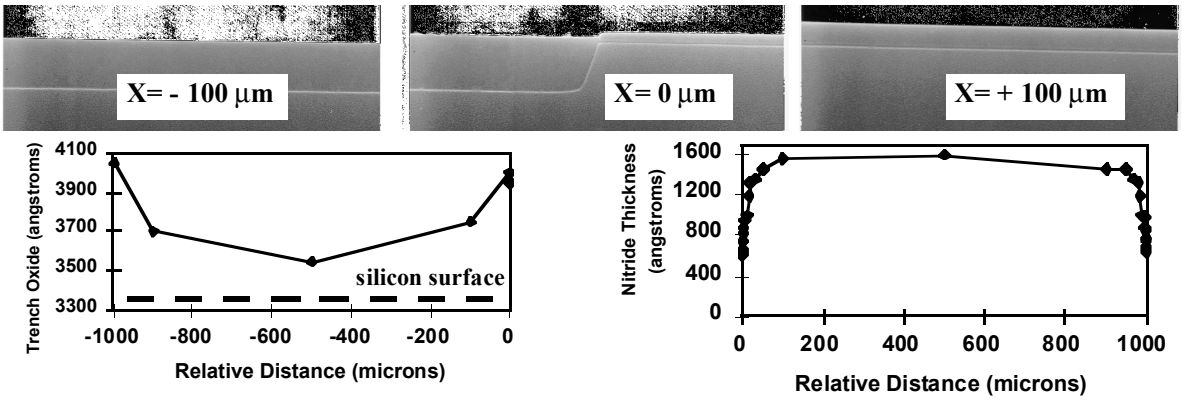

Figure 7. Trench oxide dishing and active nitride erosion across 1 mm wide trench and active feature

Similar SEM characterization was carried out on an array of 0.5 μm wide line and space with the width of the whole array equal to 1500 μm, i.e. 1500 of 0.5 μm line separated by 0.5 μm trench. This is to emulate the device layout for typical memory array. The results are shown in Figure 8, with similar polish condition and time applied to HDP and SA arrays. Due to the difference in oxide deposition profile, the "oxide" pattern density is very different between HDP STI and SA STI, as shown previously in Figures 2. As a result, the HDP array ends up with much thinner nitride remaining than SA array. Also, more edge nitride erosion occurred in the HDP array because this array was over-polished much more than the SA array due to its lower oxide pattern density. So, the optimized device layout rules for HDP should be different from that for SA. In principle, once optimized, the self-planarization feature of HDP oxide could reduce the amount of oxide deposition and, therefore, the CMP time. Both could lead to improved productivity.

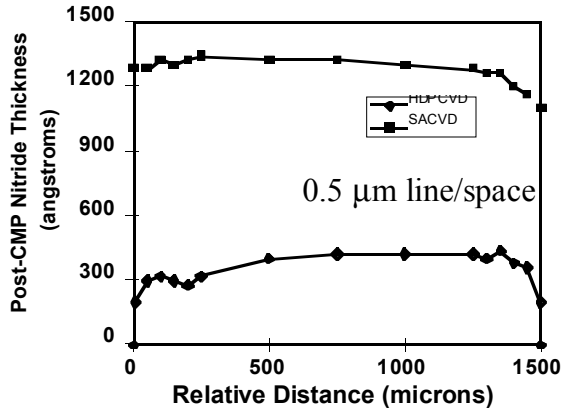

Figure 8. Different planarization behavior between HDPCVD and SACVD filled STI

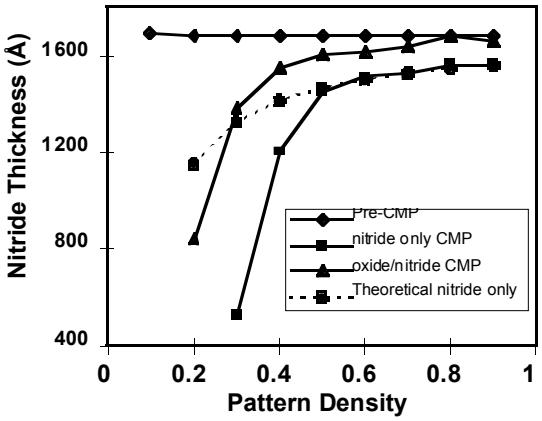

Figure 9. Selectivity degradation at lower pattern density region

Serious effort is on-going by slurry vendors to develop high selectivity slurry to improve the process window for the challenging STI CMP. It has been reported that the selectivity is as high as 200 to 1. Typically, this number is derived from polishing blank oxide and blank nitride film. To characterize the pattern density dependency of the selectivity, an etched STI wafer was polished using one high selectivity slurry without oxide trench fill. The results are shown as the "nitride only CMP" curve in Figure 9. The nitride thickness drop, or nitride CMP rate increase, toward lower pattern density is much faster than can be accounted for by pattern density only. If the nitride rate depends on pattern density only, the result should follow the "theoretical nitride only" curve. Similar acceleration of nitride rate is also observed on an oxide

filled STI wafer, as indicated by the "oxide/nitride CMP" curve. This demonstrates that the so-called high selectivity slurry starts to lose its selectivity at low active density regions. This would also explain some of the edge erosion observed in Figure 7.

CONCLUSION

Due to its stringent requirements, STI CMP has at best a very limited process window. Either additional CMP aids need to be adopted or device layout constraints need to be imposed. In either case, it is crucial that detailed characterization be carried out prior to the implementation of the specific STI planarization strategy. Additional work is planned to further investigate this subject.

REFERENCES

1. B. Stine, et al., Proc. 2nd Int. Conf. CMP for ULSI MIC, Santa Clara, CA, Feb. 1997, p. 267.
2. D. Ouma, et al., to be presented in International Interconnect Technology Conference, June 1-3, 1998, Burlingame, CA.
3. B. Davari, et al., IEDM Technical Digest, p. 61, 1989.
4. J. Boyd and J.P. Ellul, J. Electrochem. Soc., Vol. 143, No. 11, Nov. 1996, p. 3718.
5. A. H. Perera, et al., IEDM Technical Digest, p. 679, 1995.