

## **EFFECT OF FINE-LINE DENSITY AND PITCH ON INTERCONNECT ILD THICKNESS VARIATION IN OXIDE CMP PROCESSES**

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### **ABSTRACT**

The oxide polishing characteristics of fine-linewidth features typically encountered in realistic chip layouts have been examined using electrical test structures. Even at these small dimensions, we find that global pattern density plays a major role in determining the final polished oxide thickness. In addition, differences in the initial dielectric deposition profile for small features produces an apparent pitch effect which must also be taken into account. Based on experimental results, linewidth biasing during the computation of global density for modeling of CMP dielectric planarization behavior is suggested.

### **I. INTRODUCTION**

The importance of underlying topography on the polishing of interconnect interlevel dielectric (ILD) layers by chemical-mechanical polishing (CMP) is well recognized. The details of pattern dependent polishing, however, are not well understood. Previous works [1,2,3] have identified pattern density as a key factor affecting global planarization; but the definition of pattern density is often ambiguous. Furthermore, little has been reported on the effect of density for small features typically encountered in realistic chip layouts.

In this work, we examine oxide polishing characteristics over small features (down to 2  $\mu\text{m}$  pitch) and spaces in contrast to the larger features and spaces typically reported (e.g. [4]). We use electrical test structures to study ILD thickness variation over various local pattern densities and pitches; the experiments are detailed in Section II and measurement results presented in Section III. We show that, at the small dimensions, global pattern density plays the major role in determining the final ILD thickness. However, differences in the initial dielectric deposition topography for small features must also be taken into account in understanding CMP dielectric planarization behavior. Section IV discusses these results, and suggests a linewidth biasing procedure for the computation of density that accounts for the observed small line-space (narrow pitch) effect. Finally, Section V summarizes the contributions of this paper.

### **II. EXPERIMENT**

The basic test structure used to infer ILD thickness is a capacitor with a uniform top electrode and a fingered bottom electrode as shown in Figure 1a [5]. In the bottom electrode (shown in Figure 1b), we systematically vary the linewidth and spacing within the 500  $\mu\text{m}$  by 500  $\mu\text{m}$  capacitor area to explore the effects of metal pitch and local metal density (defined as the ratio of linewidth to pitch). Values of pitch explored are 2  $\mu\text{m}$ , 5  $\mu\text{m}$ , 10  $\mu\text{m}$  and 15  $\mu\text{m}$ . For each value of pitch, the line spacing and width are varied to achieve the local density values ranging from 30% to 80% in steps of 10%. This results in 24 unique capacitor structures. A 100% local density structure, consisting of a parallel-plate capacitor, is also included. Table I summarizes the experimental layout factors.

A typical probe layout consists of four different capacitor structures along with Kelvin resistors and a Van der Pauw structure which are used to account for local linewidth variation via resistive measurements (see Figure 2 (a)). The Kelvin resistors are located in the midst of dummy lines which mimic the underlying topography of the corresponding capacitor structure [5]. In order to explore the effects of global density, three replicates of each probe layout are placed within a surrounding dummy-line environment of 100%, 75% and 50% densities which are made up of 20  $\mu\text{m}$  metal pitch lines of varying linewidths (Figure 2(b)).

Six-inch test wafers each containing 48 dies were fabricated using a short-flow process. An initial PECVD TEOS layer was deposited to provide electrical isolation. A metal stack (Al:1% Cu with TiN as a barrier layer) was then deposited and patterned to form the bottom electrode of the capacitor. A thick PECVD TEOS layer forming the ILD layer was next deposited and CMP planarized down to the target dielectric thickness. After via formation, a second metal stack was deposited and patterned, forming the top capacitor electrode. ILD thickness measurements were extracted from AC high frequency (100 kHz) capacitance and linewidth measurements using lookup tables of ILD thickness versus capacitance and linewidth generated using TCAD simulations [5].

### III. RESULTS

The effect of the density in both the local structure and the surrounding environment is first considered, followed by an examination of the effect of pitch on the polishing characteristics. All final ILD thicknesses have been consistently normalized by an arbitrary constant; the lines drawn in the figures are a spline fit using the mean of the measured data points.

#### (a) Impact of the Local Density and Surrounding Dummy-Line Environment

Figure 3(a, b, c, d) shows the ILD thickness as a function of the designed local metal density; each line corresponds to one of the three surrounding dummy-line environments, and each subplot is for a specific designed pitch. As the local metal density increases, the final ILD thickness is observed to increase monotonically, except for the 2  $\mu\text{m}$  pitch case where the ILD thickness appears to be nearly constant. At each particular pitch, we also observe significant differences in the final thickness for the three dummy-line environments as shown by the pronounced separation between each line.

#### (b) Impact of Narrow Pitch

Figure 4(a, b, c) shows the final ILD thickness as a function of the local metal density; in these plots, each line corresponds to a designed pitch, and each subplot is for a specific surrounding dummy-line environment. Figure 4(b), for example, shows ILD thickness vs. local metal density in a 75% environment. We observe a linear trend for each designed metal pitch with the exception of the 2  $\mu\text{m}$  pitch structures, where the relatively constant dependence on local density is observed. Also, as can be seen from the spacing between the different lines, the sensitivity to the metal pitch value decreases for larger pitches (e.g. the difference between 2  $\mu\text{m}$  and 5  $\mu\text{m}$  pitch lines is much greater than the difference between the 10  $\mu\text{m}$  and 15  $\mu\text{m}$  lines). Similar behavior is also observed for the two other dummy-line environments (Figures 4 (a) & 4 (c)).

## IV. ANALYSIS AND DISCUSSION

### (a) Global Density Issues

Based on the results in Section III, we conclude that the polishing characteristics of a particular structure are largely a function of the combined global density of the structure and its environment. The global density is determined by an effective area of contact between the polishing pad and the layout-dependent surface topography. As seen from the plots of Figure 3, the different environments around a particular structure have a large influence on the local polishing behavior; the effective area within which the density needs to be calculated is seen to be larger than the particular structure size in our layout (500 $\mu\text{m}$  by 500 $\mu\text{m}$ ). Each structure is large enough, however, that the effective global density in and surrounding that structure is also significantly impacted (and experimentally probed) by the structure itself. We thus find that careful evaluation of the global density is necessary in order to understand the polishing behavior of an arbitrary structure within a particular environment.

A general metric for global pattern density can be defined as the ratio of metal area in a given square window to the area of the window. For this study, we calculate pattern density for a given window size from the center of a structure. Figure 5 shows the correlation ( $R^2$ ) of ILD thickness vs. a linear model of global pattern density evaluated in the given window size for all structures. Since the window is assumed to be square, its size can be represented by the length of one side of the window. The figure shows that the model correlation ( $R^2$ ) of ILD thickness and global density is maximum for a square with an edge size of 4.0mm. We thus conclude that, for this CMP process and consumable set, a 4.0mm window is an appropriate window size with which to evaluate global density from the layout for each structure. Considering the structure with line-spaces greater than 3 $\mu\text{m}$  in Figure 6, we see that a general linear trend in ILD thickness is observed as a function of the calculated combined global density using this window size.

### (b) Narrow line-space issues

In Figure 6, we see two distinct groups of structures that exhibit different dependences upon the global pattern density: those structures with line-spacing of greater than 3 $\mu\text{m}$  and those with line-spacing less than 3 $\mu\text{m}$ . We propose that this difference is due to differences in the ILD deposition profile between small and large line-space structures.

The SEM images in Figure 7 contrasts the initial deposition profile for structures with narrow line-spaces and large line-spaces. The smaller features exhibit substantial lateral deposition, resulting in a relatively flat topography compared to the larger features which have a more conformal deposition. In addition, we find that the initial step-height of the before-polish deposited dielectric film is a function of line-spacing, as summarized in Figure 8. As a result of these step-height differences, small and large line-spaces structures will have different polishing behavior. The apparent pitch/line-spacing dependence in Figures 3 and 4 is also a manifestation of these differences in the initial deposition profile. The effect of initial step-height on profile evolution can be accounted for using the model in [6]; the effect of the small line-spacings in narrow pitch features is next considered.

The impact of narrow spacings can be accounted for by an appropriate biasing in the layout linewidths prior to global density calculation; the effective bias to use can be determined from the data of Section III. In Figure 4(b), we consider first the rightmost points (70% local density) of the 2 $\mu\text{m}$  pitch lines; these have 0.6 $\mu\text{m}$  spaces which are essentially completely filled by the deposition. The 70% and 80% local density points on the 5 $\mu\text{m}$  pitch lines provide bounds on the effective lateral dimension for computational biasing of the linewidth due to deposition: the 80% points have 1 $\mu\text{m}$  spaces, while the 70% points have 1.5 $\mu\text{m}$  spaces. The 1 $\mu\text{m}$  space structures fill completely and polish the same as the 2 $\mu\text{m}$  pitch lines, while the 1.5 $\mu\text{m}$  space structures do not completely fill and polish slightly differently. For this process, an appropriate lateral bias for density computation is thus between 0.5 $\mu\text{m}$  and 0.75 $\mu\text{m}$ .

## V. SUMMARY

We have studied oxide polishing over fine pitch metal features using dedicated electrical test structures. Our experiments show that the final polished oxide thickness for a particular structure in an arbitrary surrounding may be effectively modeled as a function of global density over an empirically determined square window. The pitch/line-spacing effect observed suggests that the deposition profile shape needs to be taken into account in CMP modeling; a simple approach is to bias the linewidth during calculation of the global density. This study's results will be useful in accurate pattern dependent ILD thickness prediction, and for layout and process design optimization.

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