# Using Wafer-Scale Patterns for CMP Analysis

**Brian Lee[1], Terence Gan[1], Duane S. Boning[1], Jeffrey David[2], Benjamin A. Bonner[2], Peter McKeever[2], and Thomas H. Osterheld[2]**
[1]Massachusetts Institute of Technology, Cambridge MA
[2]Applied Materials, Santa Clara, CA

## ABSTRACT

A new set of wafer-scale patterns has been designed for analysis and modeling of key CMP effects. In particular, the goal of this work is to develop methods to characterize the planarization capability of a CMP process using simple measurements on wafer scale patterns. We examine means to pattern large trenches (e.g. 1 to 15 mm wide and 15 mm tall) or circles across 4" and 8" wafers, and present oxide polish results using both stacked and solo pads in conventional polish processes. We find that large separation (15 mm) between trenches enables cleaner measurement and analysis. Examination of oxide removal in the center of the trench as a function of trench width shows a saturation at a length comparable to the planarization length extracted from earlier studies of small-scale oxide patterns. Increase in polish pressure is observed to decrease this saturation point. Such wafer scale patterns may provide information on pad flexing limits in addition to planarization length, and promise to be useful in both patterned wafer CMP modeling and studies of wafer scale CMP dependencies such as nanotopography.

## INTRODUCTION

Current techniques for characterizing CMP typically involve patterning test dies onto a wafer, running polish experiments, and analyzing measurements to obtain characterization parameters for the process [1]. A key parameter known as planarization length is typically used to describe the length scale over which feature-induced pattern density on the wafer affects the polishing at a particular point on the die. By adding feature-scale step-height considerations to planarization length-based density evaluation, accurate models of post-CMP oxide thickness (with ~100 Angstrom error) have been demonstrated for conventional stacked pads and processes [2].

An alternative approach using wafer-scale patterns has previously shown promise as a tool to study CMP pattern dependencies [3]. With an increased interest in harder polishing pads (to increase planarization length and reduce within-die variation), the planarization length is approaching the size of the typical die. In addition, harder pads may induce a "pad flexing limit" in which the contact of the pad in large "low" regions of the die is decreased. For these reasons, as well as interest in simplified measurement and analysis of planarization length, wafer-scale patterns for detailed CMP planarization characterization are explored further in this work.
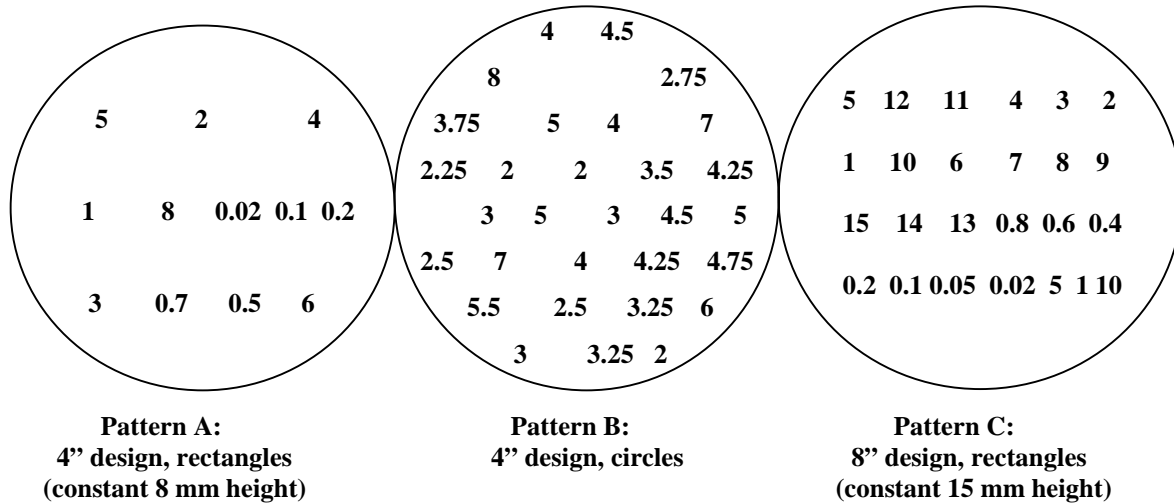
In the next section, we describe new mask designs for wafer-scale patterns. Key issues include the range of trench (or circle) sizes that should be included, as well as the separation between them on the wafer. In addition, we describe two patterning methods used here, including traditional mask plates and acetate-based masks. The following section then summarizes the sets of wafer fabrication and polishing experiments conducted, followed by analysis and discussion of the experimental results. The relationship between the observed results and previous pattern density or contact wear models is briefly considered. Finally, we offer conclusions and suggestions for further work.

## MASK DESIGN

Three sets of wafer-scale patterns are described here. Two of the designs are used for patterning 4-inch wafers, and the third design is used to pattern 8-inch wafers. The guiding principle behind the design of the masks is to fabricate structures of various sizes separated by relatively large distances to reduce interaction between these structures. The use of wafer scale patterns enables much larger structures and separations to be fabricated than is usually possible with conventional die patterns.

The layouts of the three patterns are summarized in Figure 1, where the width or diameter and relative positions of the trenches or circles are shown. The first pattern (Pattern A) is implemented as a standard quartz mask for use in a Karl Seuss contact aligner. The total pattern size is 70 mm x 70 mm, consisting of rectangular trenches 8 mm in height, ranging in width from 20 μm to 8 mm. The second pattern (Pattern B) is implemented using alternative transparency masks on 4" wafers. There are 30 circular trench structures in the layout, with 17 distinct widths ranging from 2 mm to 8 mm, and replicates of several of the structure sizes. These structures are separated from each other and from the edge of the wafer by at least 10 mm to reduce edge effects and interaction among structures. The structures are arranged in three concentric rings on the wafer. The final pattern (Pattern C) is implemented as a standard quartz mask for use in a contact aligner, with a total pattern size of 140 mm x 140 mm. It consists of 25

rectangular trench structures, each of which is 15 mm in height. There are 22 distinct widths, ranging in size from 20 μm to 15 mm, with replicates of the 1mm, 5mm, and 10mm trenches. These structures are separated from each other and from the edge of the wafer by at least 15 mm to further reduce edge effects and interaction among structures.

Pattern A:
4" design, rectangles
(constant 8 mm height)

```
   5        2         4

1      8    0.02 0.1 0.2

3    0.7   0.5     6
```

Pattern B:
4" design, circles

```
      4       4.5
   8              2.75
3.75    5    4    7
2.25  2    2   3.5   4.25
   3    5    3   4.5   5
2.5   7    4   4.25  4.75
  5.5     2.5    3.25  6
    3       3.25  2
```

Pattern C:
8" design, rectangles
(constant 15 mm height)

```
5  12  11   4   3   2
1  10   6   7   8   9
15  14  13  0.8 0.6 0.4
0.2 0.1 0.05 0.02 5 1 10
```

**Figure 1.    Mask floor plan for wafer-scale masks (dimensions in mm).**
**Positions of numbers indicate relative location of structures on the wafer.**

In addition to consideration of structure size and separation issues, in this work we investigate an alternative means of patterning wafer-scale structures. Patterns A and C are implemented using traditional mask fabrication facilities. Pattern B, on the other hand, is implemented as a lithographic print on a translucent sheet of acetate (i.e., transparency), which is then used in a Karl Seuss contact aligner to pattern wafers. The lithographic print method is chosen to insure sufficient opaqueness of the pattern. This method results in poor structure edge resolution, and restricts the minimum structure size on the mask to 2 mm.  For the study of large scale polishing behavior (large multi-mm structures), these limitations are not critical. The benefit of this method is that it enables inexpensive and rapid production of distinct wafer-scale patterns for characterization work.

## EXPERIMENTAL DETAILS

Pattern A and Pattern B wafers are polished on a Strausbaugh 6EC CMP tool using a standard pad stack (IC1000/SubaIV) and slurry (Cabot SS-12). Pattern C wafers are polished on an Applied Materials Mirra[TM] tool using standard and harder pad stacks and standard slurry.

Pattern A wafers have 1.5 μm of CVD oxide, and are patterned and etched to produce 0.6 μm trenches using a wet etch process. The wafers are then polished under the following process conditions: 25 rpm table speed, 55 rpm quill speed, 3 psi down force, 1 psi back pressure, modifying the polish time to yield splits of three different thickness removals: 0.4 μm, 0.6 μm, and 0.8 μm.

Pattern B wafers have an initial CVD oxide of 1.5 μm, and are patterned (using the alternative mask method), and then etched to produce 0.7 μm trenches using a wet etch process. The wafers are then polished under the following process conditions: 25 rpm table speed, 15 rpm quill speed, 2.5 psi down force, 1 psi back pressure, modifying the polish time to yield splits of three different thickness removals: 0.3 μm, 0.5 μm, and 0.7 μm.

Pattern C wafers have trenches etched in silicon to an etch depth of 0.82 μm, with 1.5 μm of oxide then deposited across the wafer. Wafers are polished under three different process conditions (constant speed and varying pressures), but all splits are targeted towards the same amount of oxide removed (0.5 μm).

Thickness measurements are taken across the trenches using standard profilometry scans (in Pattern A), optical measurements (in Pattern B), or high-resolution optical measurements (in Pattern C).

## EXPERIMENTAL RESULTS

One proposed method of using wafer-scale post-polish measurement data to characterize the CMP process is to analyze the amount of material removed in the center of trench structures as a function of the structure size. Wider trenches should result in more material removed, since the CMP pad can deform into the trenches to a greater de-

gree. In this section, we examine the polish data from the trench structures of different sizes. Results indicate that wafer scale uniformity, as well as structure separation, are important considerations for wafer scale patterns. Given sufficient separation, trends in trench removal vs. structure size are clearly discernible.

**Polish Depth and Structure Separation Guidelines**

As expected, the amount of trench oxide removal increases as the etched structure size increases, as shown in Figure 4 for Patterns A and B. We see that the curve for Pattern B (which uses a non-traditional patterning step and circular trenches) exhibits the same general signature as the curve for Pattern A (which uses a traditional patterning step and rectangular trenches). Figure 4a shows that the general signature of the process does not change with the amount of material removed (approximately scaling with amount removed), provided that one does not polish past the depth of the trench itself. The curve for the 0.4 μm and 0.6 μm target removals show similar signatures, while the curve for the 0.8 μm removal exhibits a much noisier signature. We conjecture that wafer scale polish nonuniformities are exacerbated or that trench structures interact more strongly for large material removals, suggesting that moderate amounts of polish are best for wafer scale pattern studies.

Figure 4b shows the trend of trench area removal vs. structure size for the Pattern B wafers, where structures are replicated in three concentric rings on the wafer. We see that the general range of values and curve trends do not change depending on ring position. However, the structures nearer to the edge seem to exhibit a much noisier signal than the structures in the center of the wafer. Here again the 10 mm separation distance between structures and from the edge of the wafer may not be sufficient to block against structure interaction. The potential for wafer scale polish uniformity to affect structure polish also suggests that replication of trench structures is important in order to separate polish uniformity from trench size dependencies.

**Pad and Process Impact on Trench Removal vs. Trench Width**

Pattern C wafers, consisting of structures with larger 15 mm heights and separations, are polished using two different pads and three different polish processes; the trench removal vs. trench width plots are shown in Figure 5. The left side of Figure 5 shows results using a standard stacked pad, while the right side plots the results with a hard polishing pad. Three polishing processes in which only the head pressure varies are shown from top to bottom, where increasing pressure is from curves (a) to (c) and from curves (d) to (f).

Considering first the standard standard stacked pad and process of Figure 5(a), we see that the trench removal reaches a saturation point for trench sizes in the 5-6 mm range, at which point the trench removal is nearly constant (but less than in the surrounding unetched regions) for increasing trench widths. We also see that the trench removal appears to linearly decrease toward zero for smaller trench widths. As the polish pressure increases from Figure 5(a) to (c), we see that the saturation point becomes more pronounced and appears to occur at smaller trench widths. The difference between the trench and non-trench oxide removal for the largest trench sizes also decreases for the larger pressure processes.

Comparing these stacked pad results with the hard pad results shown in Figure 5(d) to (f), we see a dramatic difference in the saturation point for the harder pads. Indeed, for the lower pressure the saturation point is not reached for the largest 15 mm structure examined here. In the case of the highest pressure process, we see what may be a fairly sharp saturation at a trench width of 15 mm, compared to 4-5 mm for the stacked pad at the same pressure. For study of emerging hard pad CMP processes, these results suggest that wafer scale patterns with even larger structures and separation distances should be considered in the future.
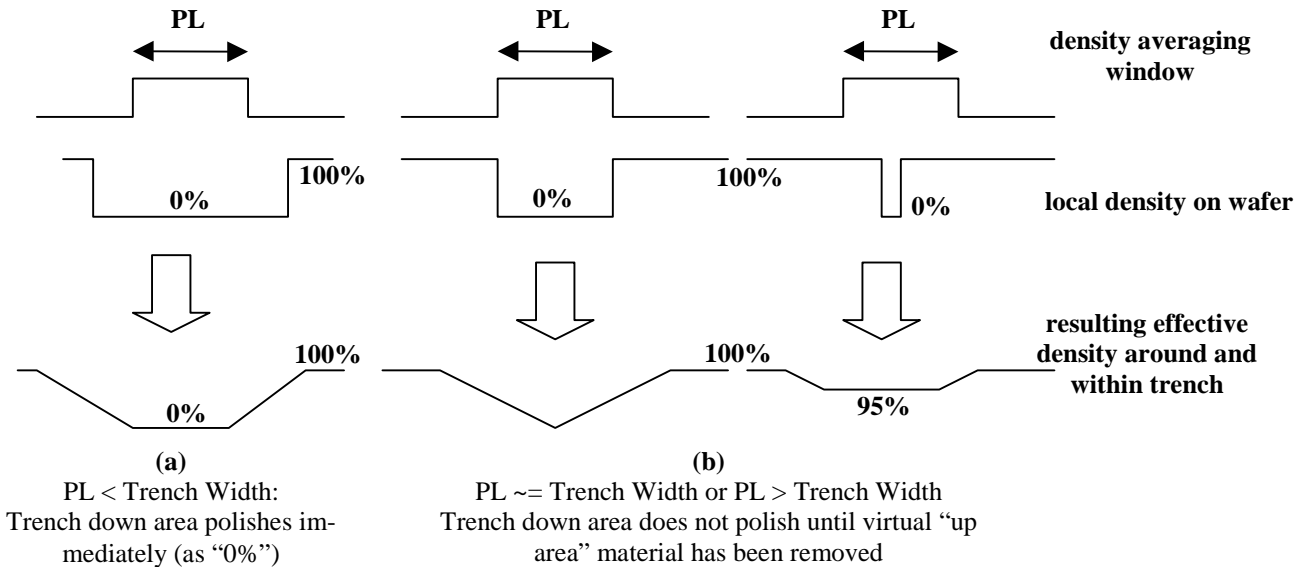
## DISCUSSION AND MODELS

In this section, we first consider the relationship between the observed data and a pattern density-based CMP model, and then briefly consider the above data from the perspective of a contact wear model.

**Planarization Length and Pattern Density-Based Model**

The "planarization length" is used to describe the ability of a CMP process to remove variation on a die [1]. The saturation point on the curve for the standard pad is in the 4-6 mm range, which is comparable to planarization lengths previously extracted for this process using pattern density test masks [4]. An idealized pattern density-based CMP model is considered here to show that this saturation point is the same as the planarization length parameter.

Figure 2 illustrates the trench polish problem using an idealized analysis, in which a simple square averaging window of size equal to the planarization length is used to calculate the "effective density" of raised topography around and within a trench. The effective density as calculated as the ratio of raised material to total area within some region defined by the planarization length. The effective density-based polish model assumes that raised or

"up" areas of regions will polish as the blanket rate divided by the effective density of that region, and once the up structures are removed the region polishes at the blanket polish rate [1].



**(a)**
PL < Trench Width:
Trench down area polishes immediately (as "0%")

**(b)**
PL ~= Trench Width or PL > Trench Width
Trench down area does not polish until virtual "up area" material has been removed

**Figure 2.    The trench polish problem using a planarization length (PL) and effective density analysis.**

We see in Figure 2 that trenches with widths larger than the planarization length of the process have a trench central region that polishes as a "0% effective density area" surrounded by areas of monotonically increasing density. Regions more than half a planarization length away from the trench edge polish as 100% effective density regions (or at the blanket polish rate). In the "0% effective density area" the wafer should polish as the blanket rate. For trenches with lengths equal to or less than the planarization length, the trench central region will evaluate to a non-zero effective density, so that no down area (i.e. trench center) polish occurs until the up area material is removed. For the trench case where we have non-zero density points inside the trench, this would refer to virtual "up area" since points inside the trench have no real up area material. The hypothetical trench removal vs. trench width plot resulting from this effective density polish model is summarized in Figure 3.

While the effective density models can relate the saturation point in the plots of Figure 5 to the notion of planarization length, other aspects of the data are not well explained using such a model. First, as discussed earlier, at saturation the trench removal amount is less than the corresponding amount removed from outside of the trench, while the density model suggests they should both polish at the blanket rate (the dashed line in Figure 3(a)). Second, the data for both the standard and harder pads indicate that trench down area removal is zero only at very small trench sizes, while the density model predicts a substantial range of zero polish. Down-area polish before complete removal of local step height has been modeled [2; however, the step height at which this begins to occur (e.g. 2000 Angstroms) is less than the final trench height in this polish experiment. The polish results presented here may indicate that such step "contact heights" may be very large for such large structures.

## Contact Wear Model

Since the effective density/planarization length approach was originally formulated consider polishing on the feature scale, an alternative method of analysis may be more suited for approaching the macroscopic wafer-scale polishing problem – that of considering pad/wafer contact mechanics [5,6]. This approach considers the physical interaction of the contact between an elastic pad and the wafer, and forms a relationship between the displacement of the pad and the pressure on the wafer. We implement a contact mechanics model similar to that in [5,6] and apply the model to the trench polish problem resulting in a hypothetical trench removal vs. trench width curve as shown in Figure 3(b). Using a contact mechanics argument, the pressure on the pad at the bottom of a trench is less than the pressure on the raised area, which directly translates to less material removed in the trench center than on the area outside the trench, thus explaining that characteristic of the observed data. The contact mechanics approach can also

result in zero down polish for non-zero trench widths (i.e. there may be a width at which the pad does not contact the wafer). This aspect of the data observed in Figure 4 needs further exploration.



(a) Curve for effective density model



(b) Curve for contact wear model
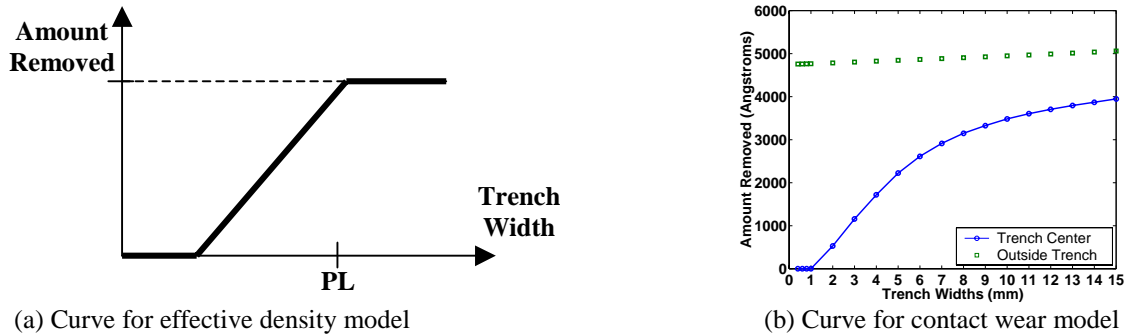
**Figure 3.    Hypothetical amount removed vs. trench width plots, for pattern density-based model (a), and contact wear model (b).**

## CONCLUSIONS

We have examined wafer-scale patterns as an alternative means for characterizing and modeling CMP processes. Polishing results suggest that such wafer scale patterns benefit from very large separations of structures from each other and the wafer edge to avoid interactions, particularly for harder pad or longer planarization length processes.  Trench removal vs. trench width plots provide useful insight into the polish process, and can indicate a planarization length parameter.  Such plots also reveal dependencies that merit further exploration (the difference between large trench and outside trench polish, the width at which trenches begin to polish) using contact mechanics and other modeling approaches. Future models of CMP pattern evolution may well require integration of both macroscopic consideration and feature scale behavior.

Wafer-scale pattern experiments and modeling may prove particularly useful in the study of "nanotopography" or "nanotopology" related to the nanometer-scale surface variations (occurring over mm length scales across the wafer) that may be present on bare silicon wafers [7]. It has been proposed that natural "random" nanotopography that occurs on an unpatterned raw silicon wafer can be approximated by using a fixed grid of randomly sized cylindrical posts on a wafer-scale pattern [8]. Polishing of such patterned films could lead to insights on how to model the CMP of natural nanotopography on wafers.

## ACKNOWLEDGMENTS

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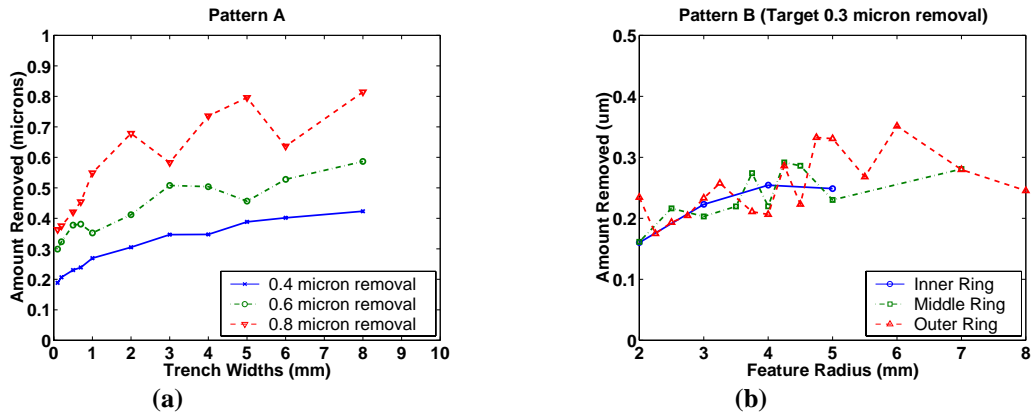
**Figure 4.    Trench removal vs. structure size for Patterns A and B.**
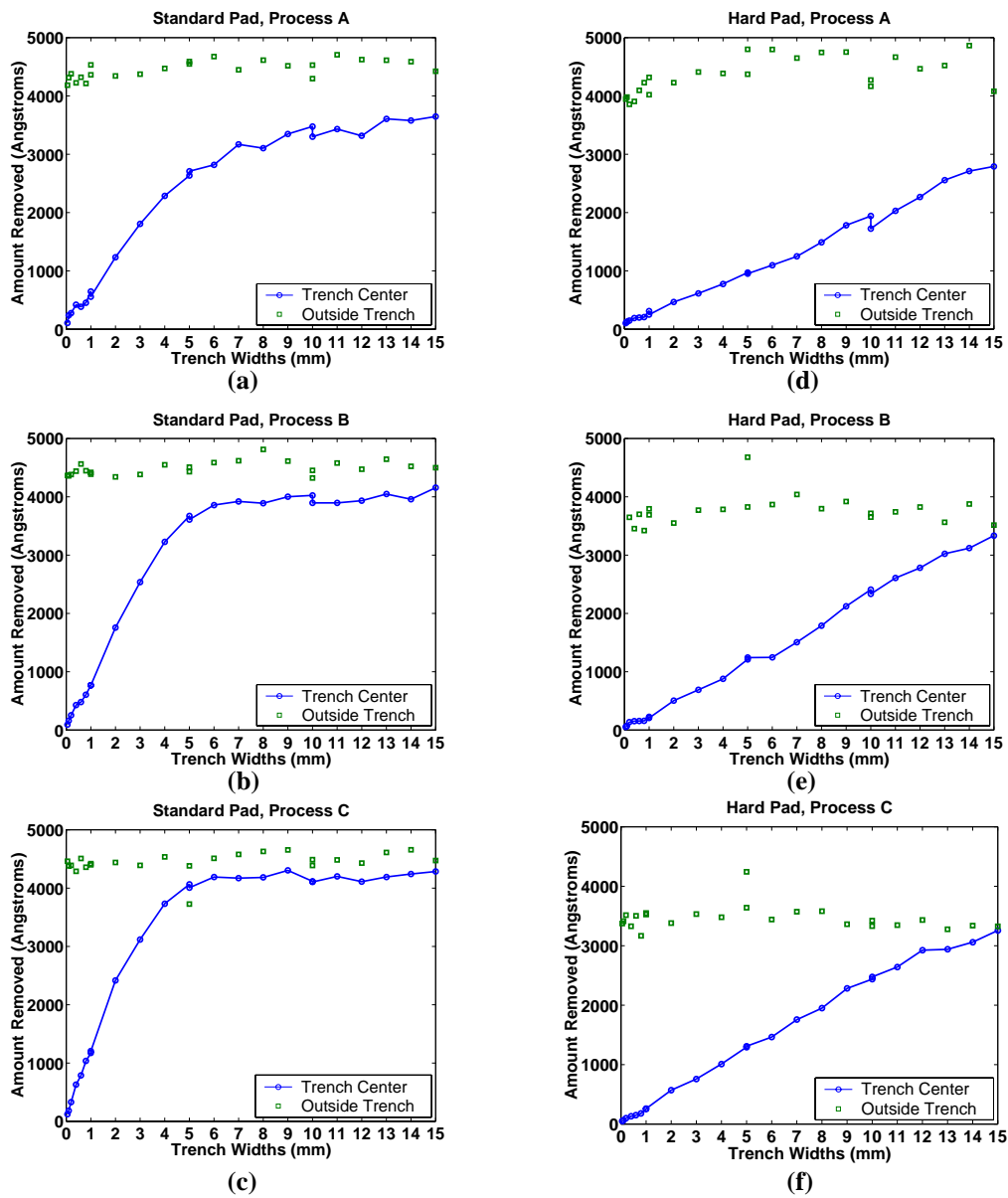
**Figure 5.    Amount removed (center & outside) vs. trench width, Pattern C.**