Characterization and Modeling of Nanotopography Effects on CMP

Prof. Duane Boning, Brian Lee
Microsystems Technology Laboratories
Massachusetts Institute of Technology, Cambridge, MA

Win Baylies*, Noel Poduje, Pat Hester
Baytech Group*, ADE Corp.

John Valley, Chris Koliopoulos
ADE Phase Shift

Dale Hetherington, Sandia National Labs

boning@mit.edu, phone: 617-253-0931
http://www-mtl.mit.edu/Metrology

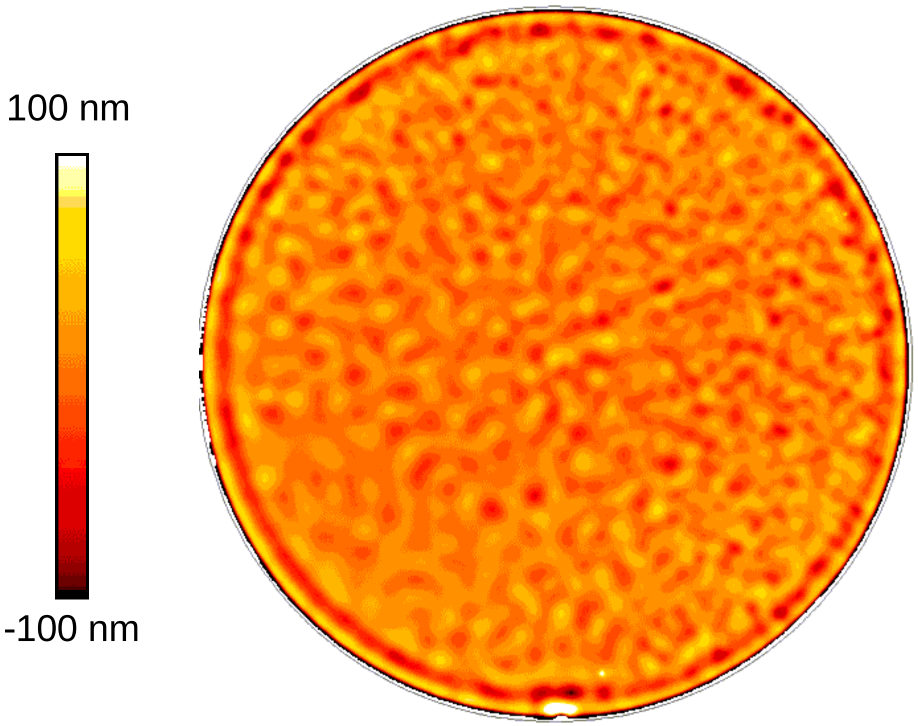
Outline

1. What is Nanotopography?
    - Effect of nanotopography during CMP
2. CMP Planarization Length
    - Hypothesis: CMP planarization length (PL) determines how thin films over nanotopography evolve during polishing
3. Modeling of Nanotopography Effects During CMP
4. Nanotopography/CMP Experiments
    - Process and measurements
    - Wafers: range of nanotopography features/length scales
5. Experimental results
6. Nanotopography and STI CMP
7. Conclusions

What is Nanotopography?

"Nanotopography" refers to wafer surface variations with:

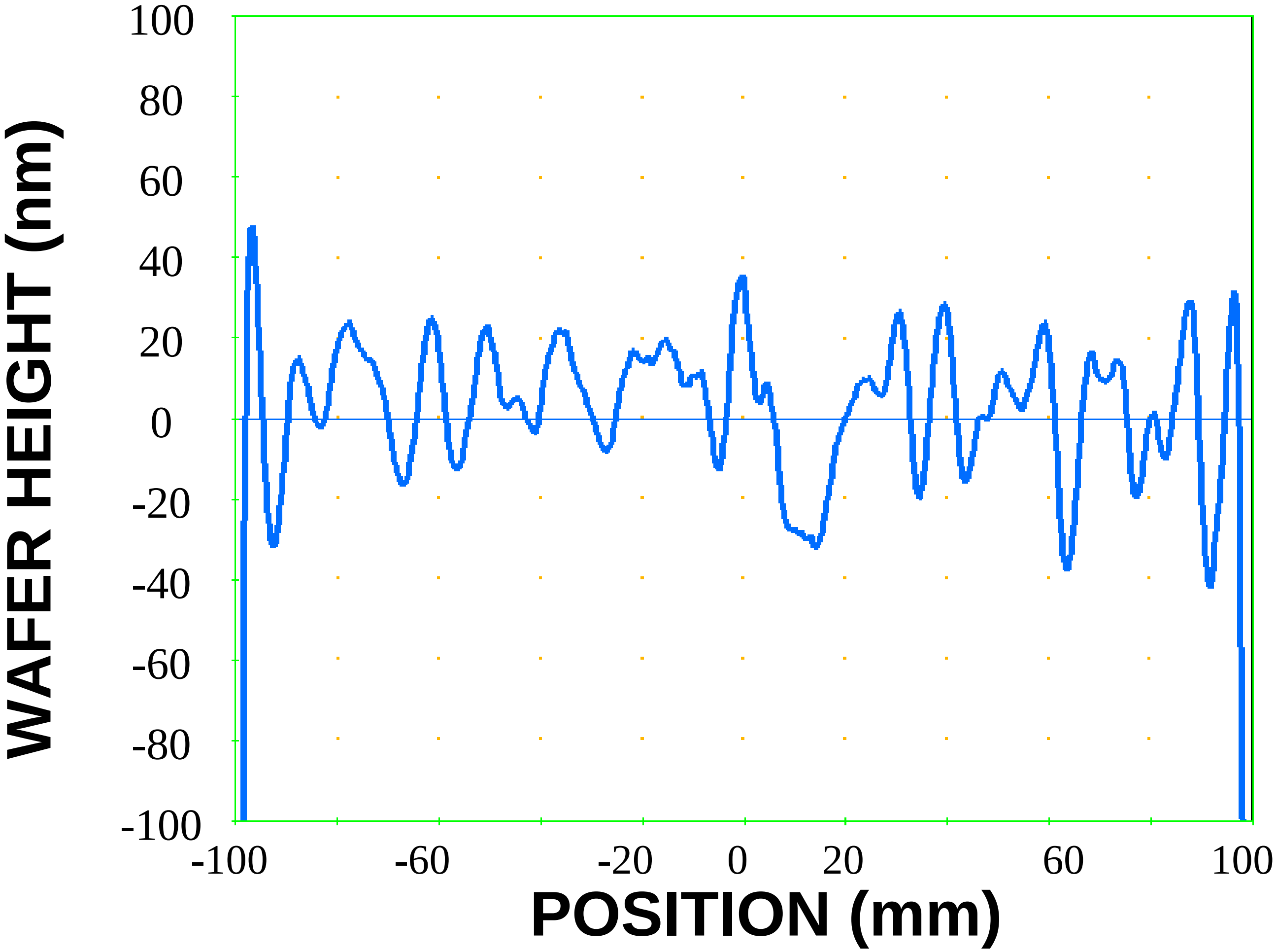
1. Lateral length scales from 0.2 mm to 20 mm
2. Height variations ~ 10 to 100 nm



Nanotopography Map:
8" SSP Silicon Epi Wafer

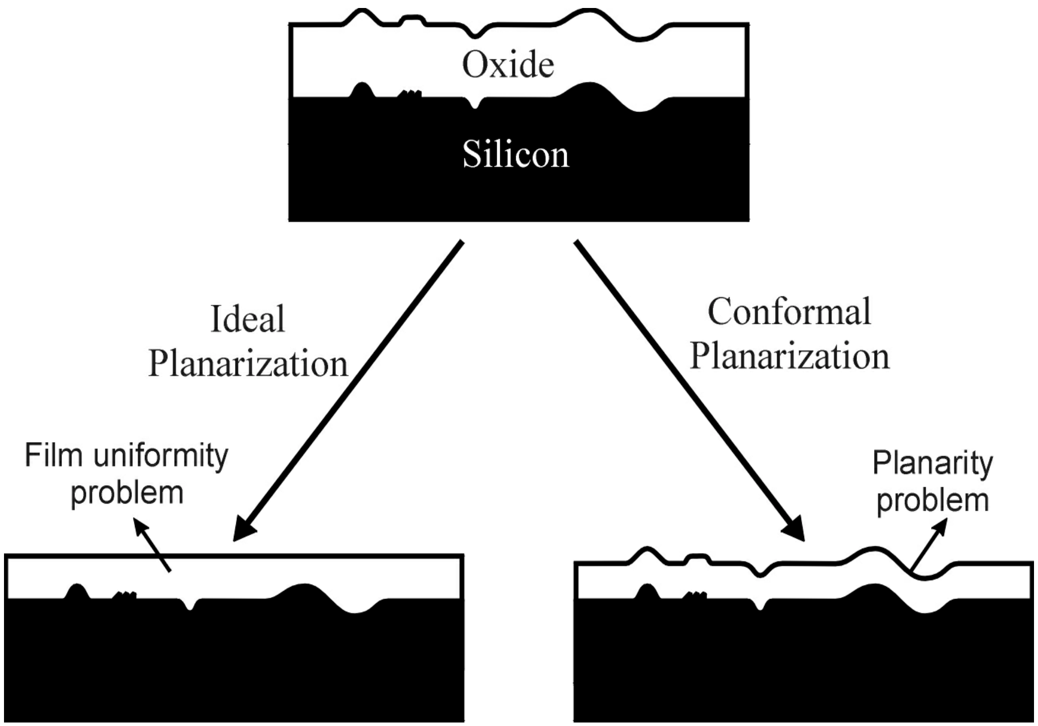
Filtered data measured using a NanoMapper™ production nanotopography tool at ADE Phase Shift in Tucson, AZ

SSP wafer, Diameter Scan (Filtered Data) using NanoMapper^{TM}



*Measured using a NanoMapper™ production nanotopography tool at ADE Phase Shift in Tucson, AZ

Nanotopography Propagation During CMP



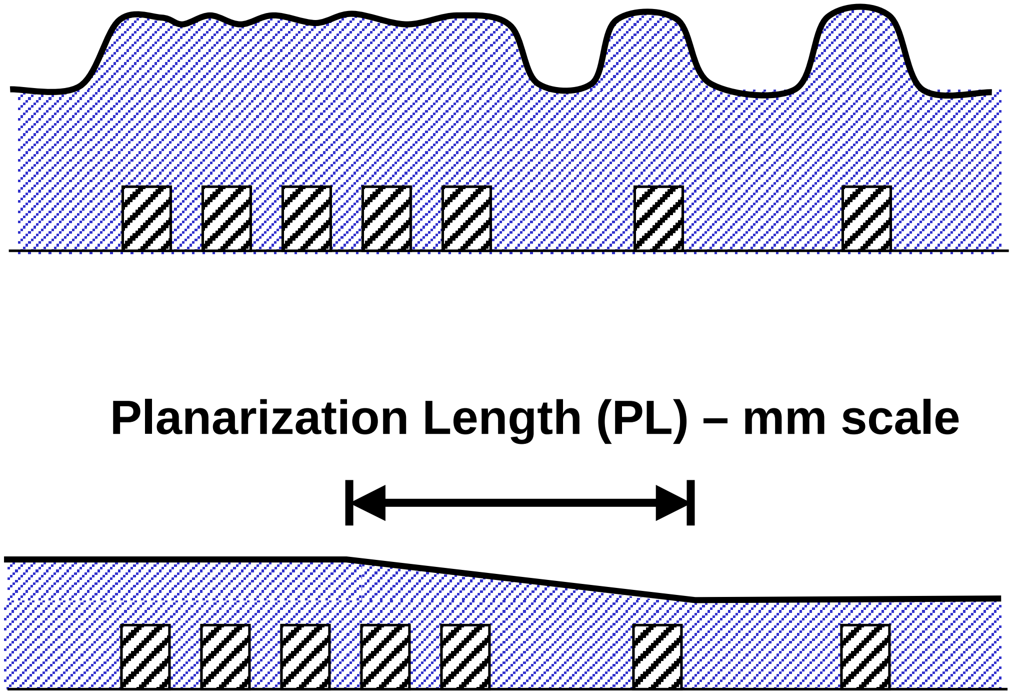
Xu *et al*, Electrochemical and Solid-State Letters, **1**, 181, 1998.

- Conformal Polishing
  - Observed with “soft” pads
  - Oxide thins uniformly
  - Nanotopography propagates as variation in ***surface height***
  - ⇒ Lithography concern
- Ideal Planarization
  - Observed with “stiff” pads
  - Nanotopography propagates as variation in ***final oxide thickness***
  - Flat surface
  - ⇒ STI yield concern

2. CMP Planarization Length

Planarization of Dielectrics in Conventional CMP

- CMP achieve good local planarity (µm scale features)
- CMP creates global non-planarity (mm scale regions)



Pre-CMP

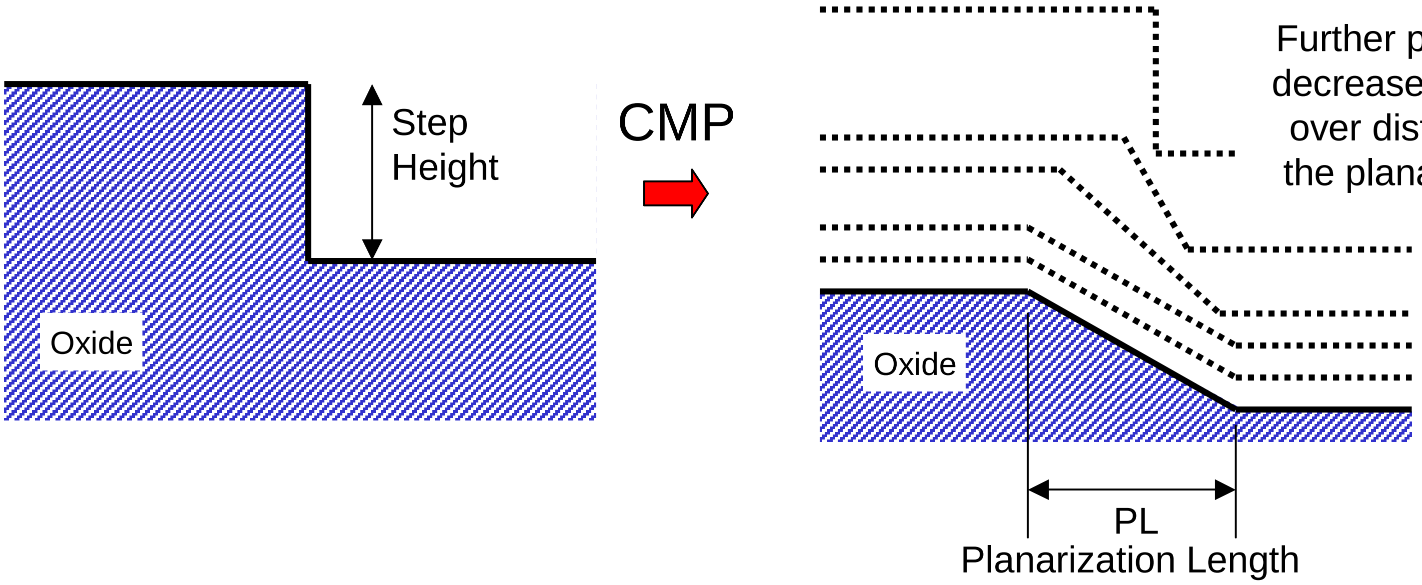
Planarization Length (PL) – mm scale

Post-CMP

▨ **Oxide**

▨ **Metal Lines**

CMP Planarization Length



Further polishing cannot decrease the step height over distances beyond the planarization length

Planarization Length

- Planarization length (PL) is strongly influenced by the polishing pad
  - intuition: PL as "flexing distance" of the pad/process
- PL also influenced by other parameters:

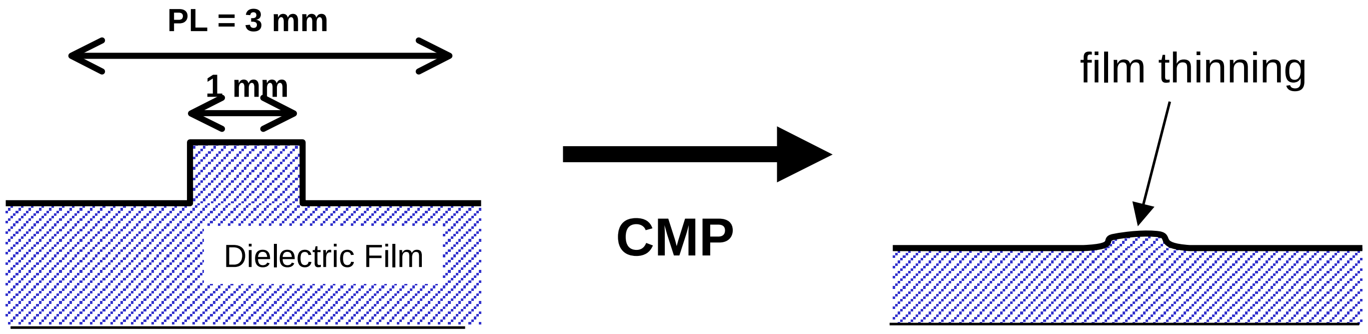
$$PL = \boldsymbol{f}\,(\text{pad, slurry, process, tool, ...})$$

where the details of the function ***f*** are not yet well understood

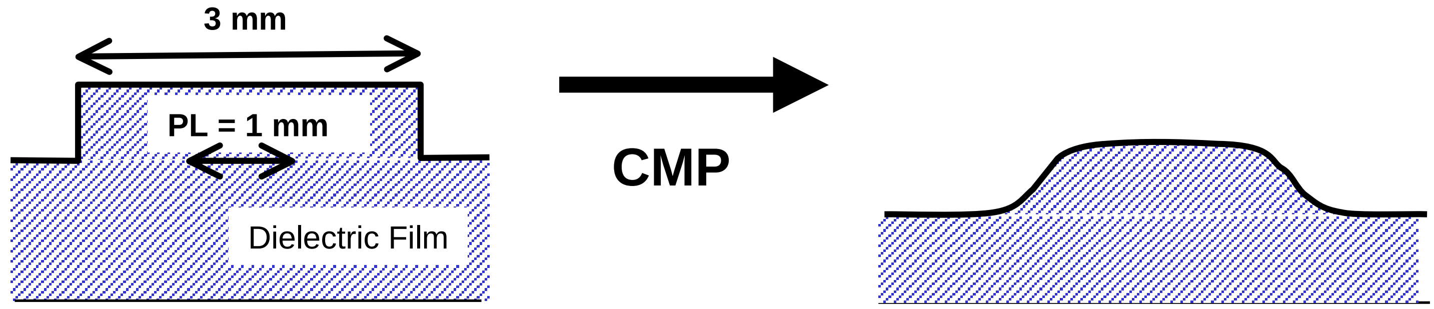
- PL *characterizes* the planarization capability of the CMP process
  - one *measures* PL by polishing special test wafers

Planarization Length Implications

- For structures less than planarization length (PL) ⇒ planarization (thinning) occurs

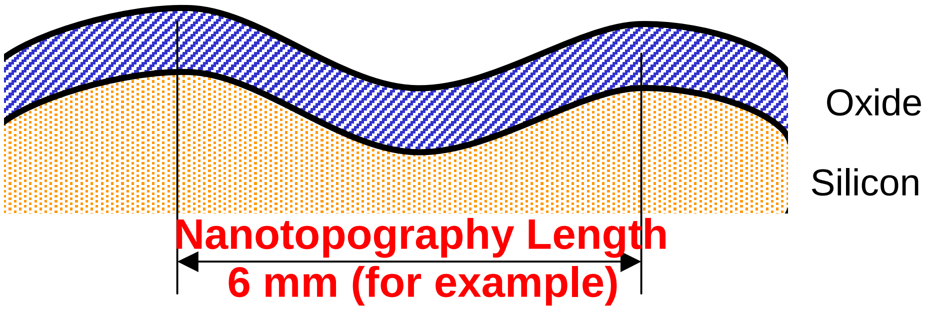


- For structures larger than planarization length ⇒ surfaces polish together; little or no planarization



Nanotopography & Planarization Length

Given nanotopography variations on some length scale...

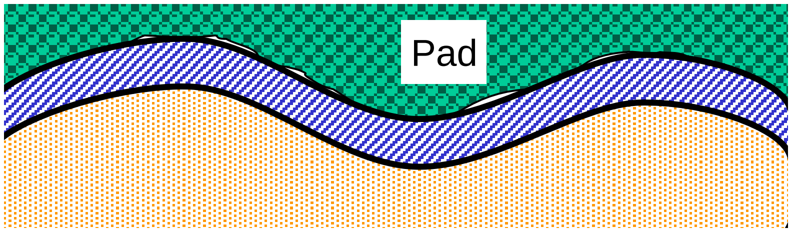


What happens during CMP?

CMP

"Soft" Pad CMP Process

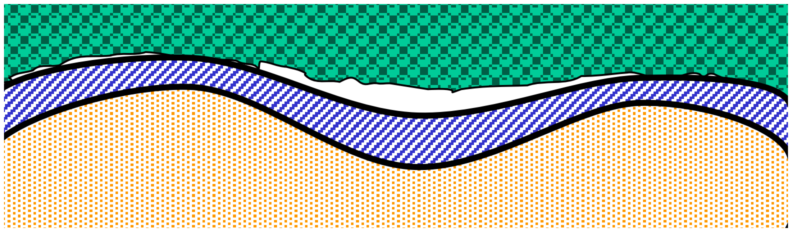
Planarization Length ~ 3-4mm



- pad conforms around nanotopography variations and polishes uniformly

"Stiff" ("Hard") Pad CMP Process

Planarization Length ~ 7-10 mm



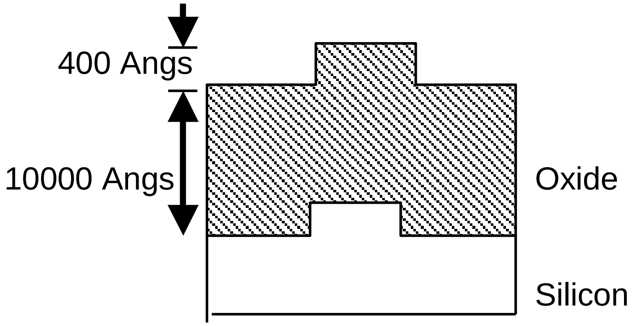
- pad "bridges" across nanotopography down areas and preferentially thins surface films in raised nanotopography areas

3. Simulation of Nanotopography CMP

Nanotopography Modeling Methodology

Simulate initial nanotopography as grid of structures

Cross Section



Use CMP models to simulate polish

density/step-height CMP model

contact wear CMP model

Compute thinning

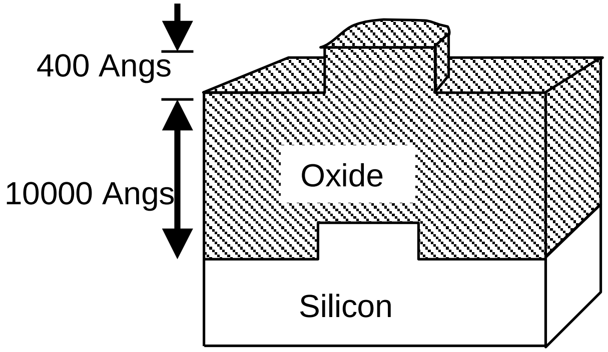
Define *nanotopography length* (NL) as the grid spacing of structures; this correlates to the lateral distance between nanotopography features on a wafer

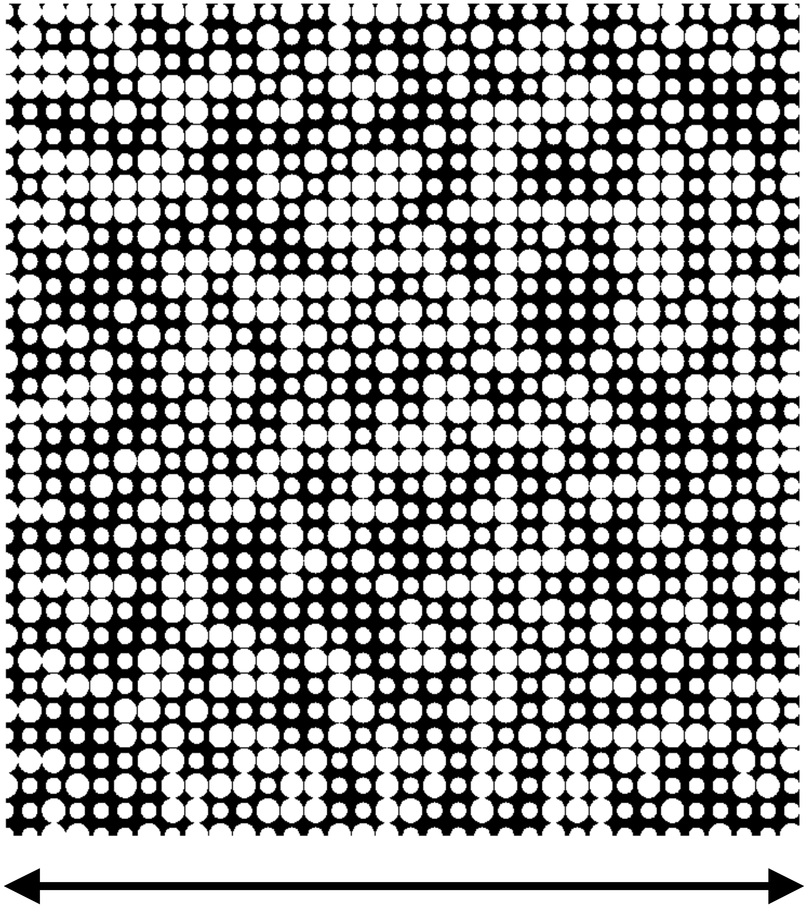
Hypothesis: NL < PL => significant thinning
NL > PL => no (or minimal) thinning

Modeling Wafer Surface Nanotopography

Create a millimeter-scale grid and populate with cylindrical posts of random, millimeter-scale diameters. All posts have a height of 400 Angstroms. Assume an initial field oxide thickness of 10000 Angstroms

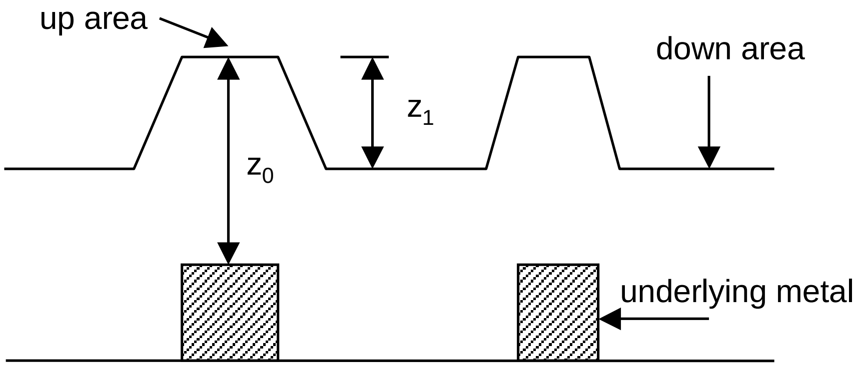
Cross Section





CMP Film Thickness Evolution Model (I)

Density/Step-Height based CMP model[1,2]



$RR_u = K/\rho$; $RR_d = 0$ $\quad t < t_c$

$RR_u = K + (1-\rho)*(h_c/t)*\exp(-(t-t_c)/t)$ $\quad t > t_c$

$RR_d = K - \rho*(h_c/t)*\exp(-(t-t_c)/t)$

K: blanket film polish rate
z_1: initial step height
z_0: initial film thickness
t: time constant

ρ: effective feature density
h_c: contact height
t_c: contact time
t: polish time

Key ideas:

- Local removal rates in the raised areas are weighted by the *effective feature density*
- Local removal rates in raised and down areas exponentially change in time after a certain *contact height* is reached (which occurs at a *contact time*)
- Removal rates of raised and down areas converge to blanket removal rate over time

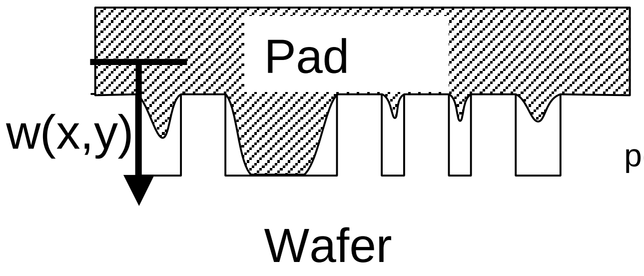
---

[1] Brian Stine, et al.,"A closed form analytic model for ILD thickness variation in CMP processes," *Proc CMP-MIC*, Feb. 1997.

[2] Taber Smith, et al., "A CMP model combining density and time dependencies," *Proc. CMP-MIC*, Feb. 1999.

CMP Film Thickness Evolution Model (II)

Contact Wear CMP Model[1,2]



Pressure-displacement equation

$$w(x,y)=[(1-\nu^2)/(\pi E)]\int p(\xi,\eta)*[(x-\xi)^2+(y-\eta)^2]^{-1/2}\,d\xi d\eta$$

$w(x,y)$ = displacement of pad at (x,y)

ν: Poisson's ratio

$p(x,h)$ = pressure of pad on wafer at (x,h)

E: Young's modulus

Preston's equation

$$RR\ (x,y)= K_p*p(x,y)*v(x,y)$$

RR: film removal rate

$p(x,y)$: pressure

K_p: Preston's coefficient

$v(x,y)$: velocity

Key ideas:

- Use pressure-displacement equation to solve for pressures everywhere
- Use Preston's equation to calculate removal rates
- Advance boundary elements, and iterate to reach desired polish time

[1] O. G. Chekina, et al., "Wear-contact problems and modeling of chemical mechanical polishing," *JECS*, Vol 145, June. 1998.

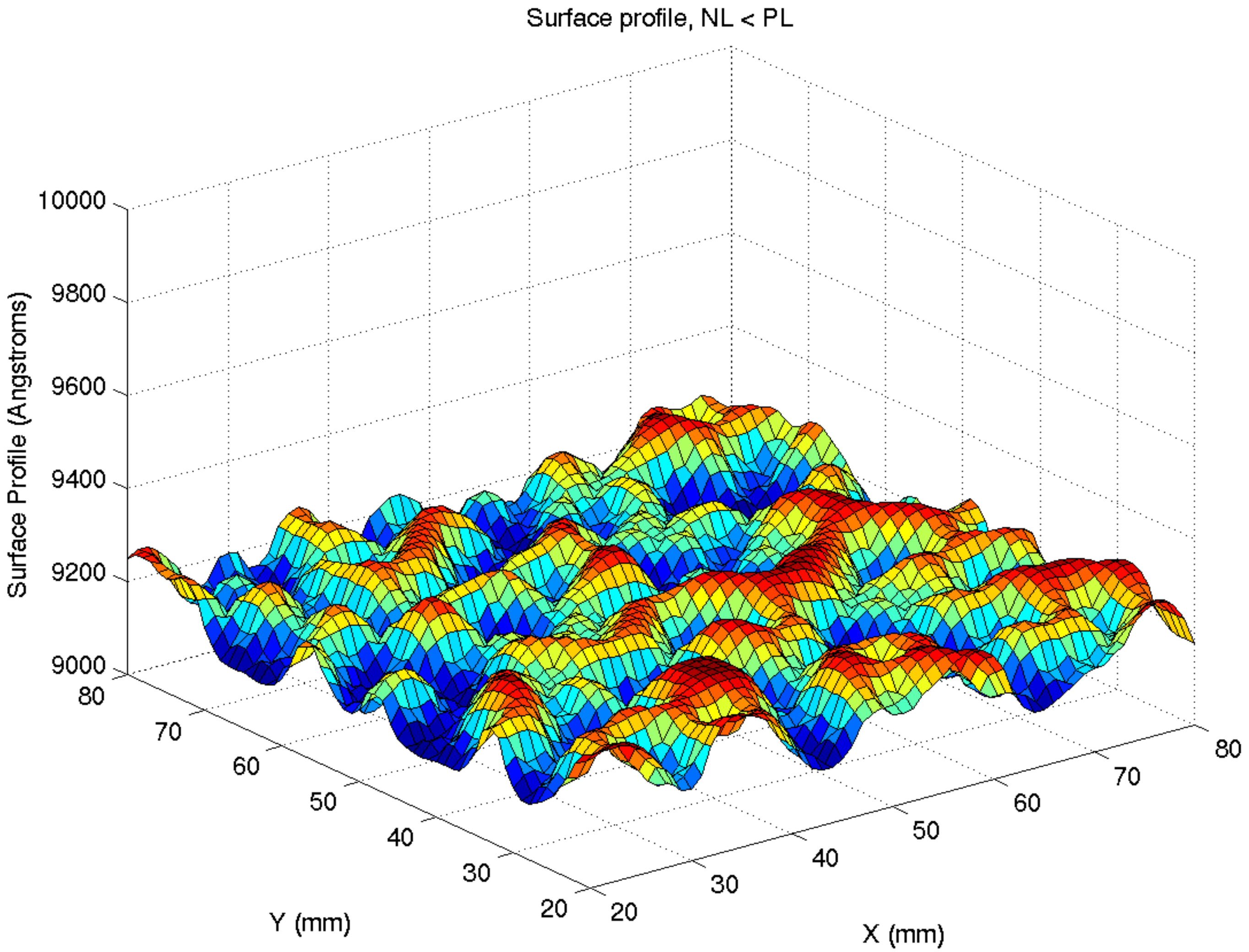
[2] T. Yoshida, "Three-dimensional chemical mechanical polishing process model by BEM," *ECS Conf.*, Oct. 1999.

Simulation Parameters

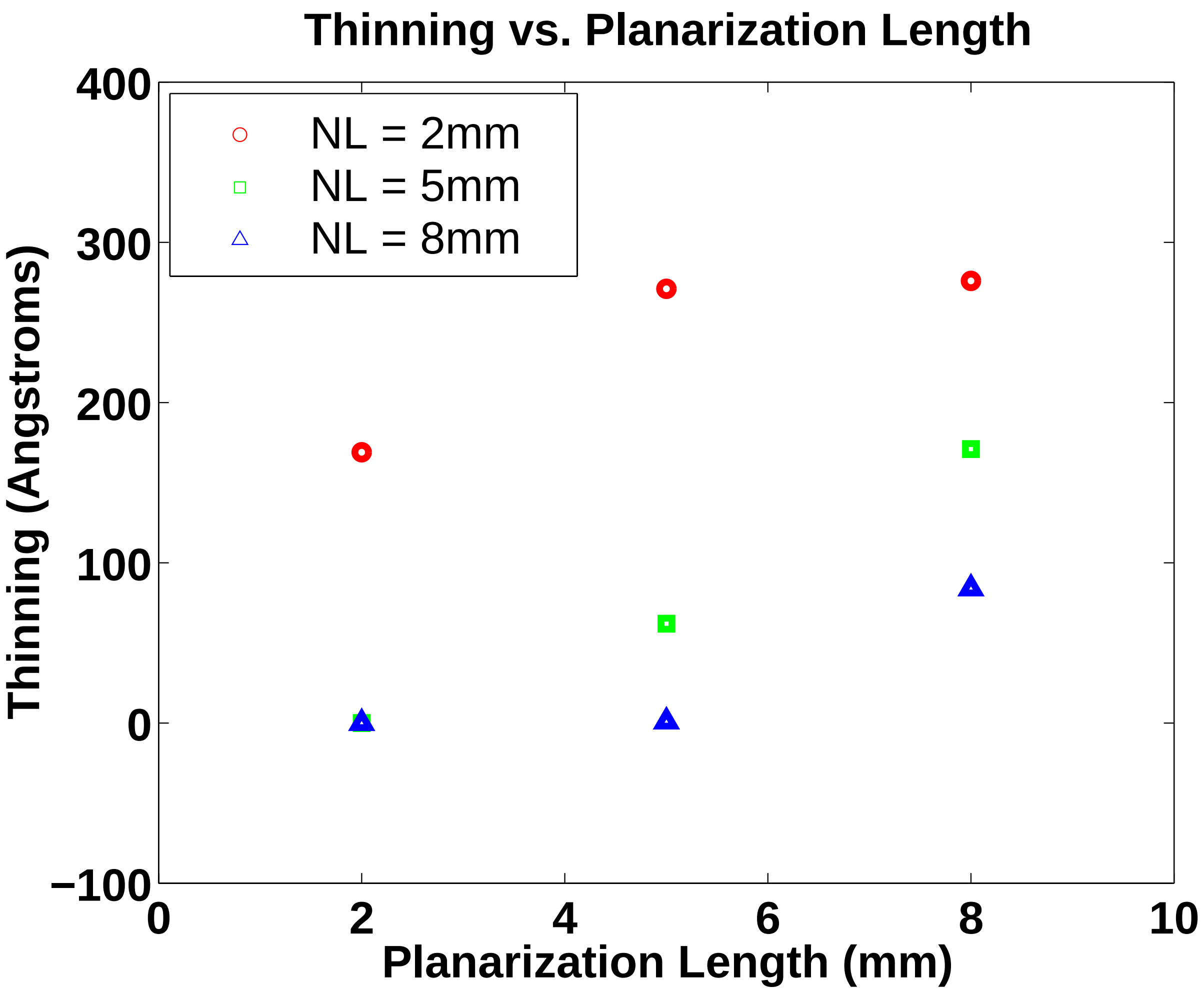
- Pre-CMP oxide thickness variation: 0 Angstroms
- Pre-CMP Step Height = 400 Angstroms
- Initial Thickness = 10000 Angstroms
- 60 second polish
- Three nanotopography lengths: 2, 5, 8 mm
- Density/Step-Height model: three planarization lengths (2, 5, 8 mm)
- Contact Wear model: three Young’s moduli (72, 147, 294 MPa)

- ***Hypothesis: Significant oxide thinning occurs when nanotopography is on a shorter scale than the planarization length***
- ***Hypothesis: Thinning increases with stiffer pads***

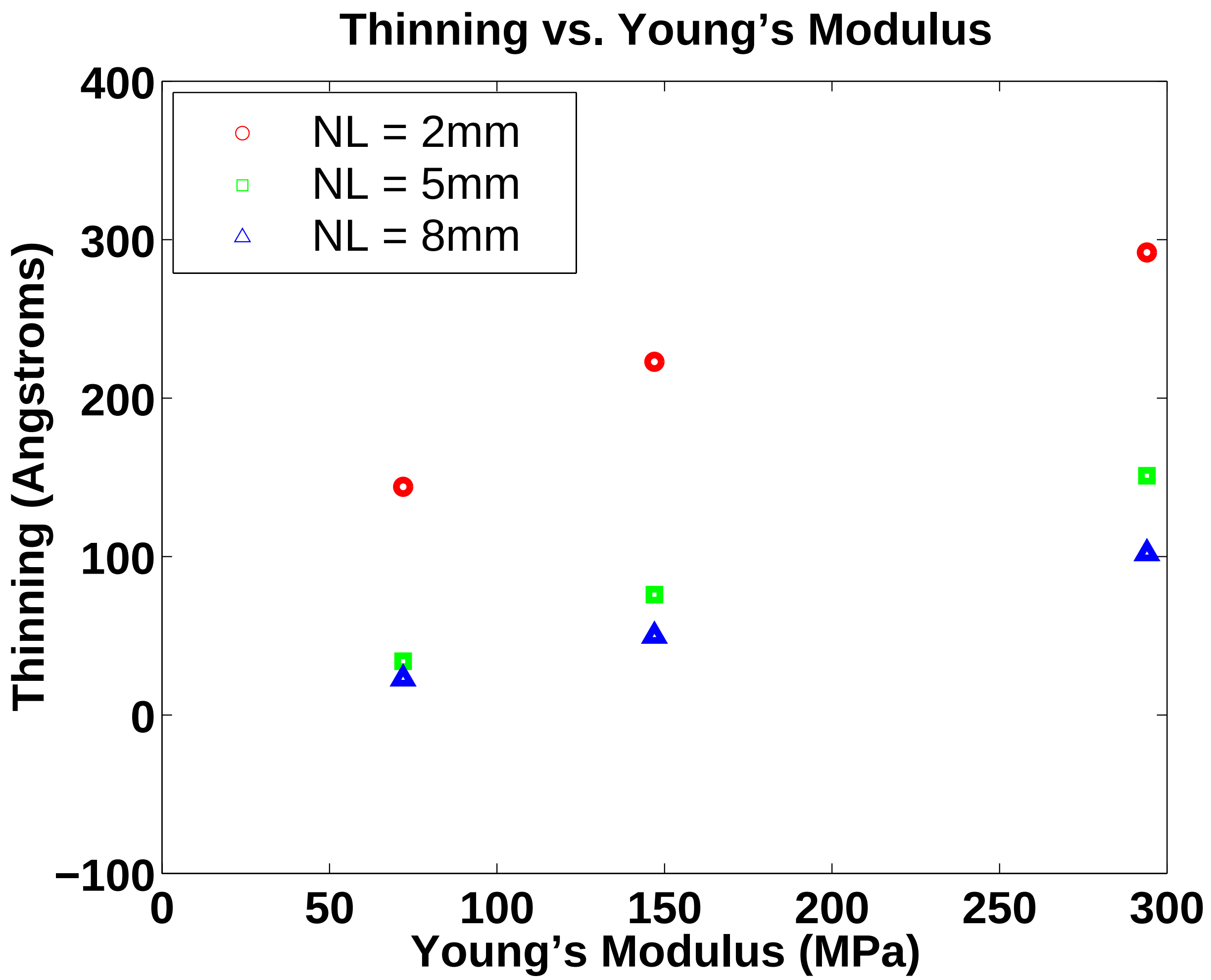
Simulated Post-CMP Surface



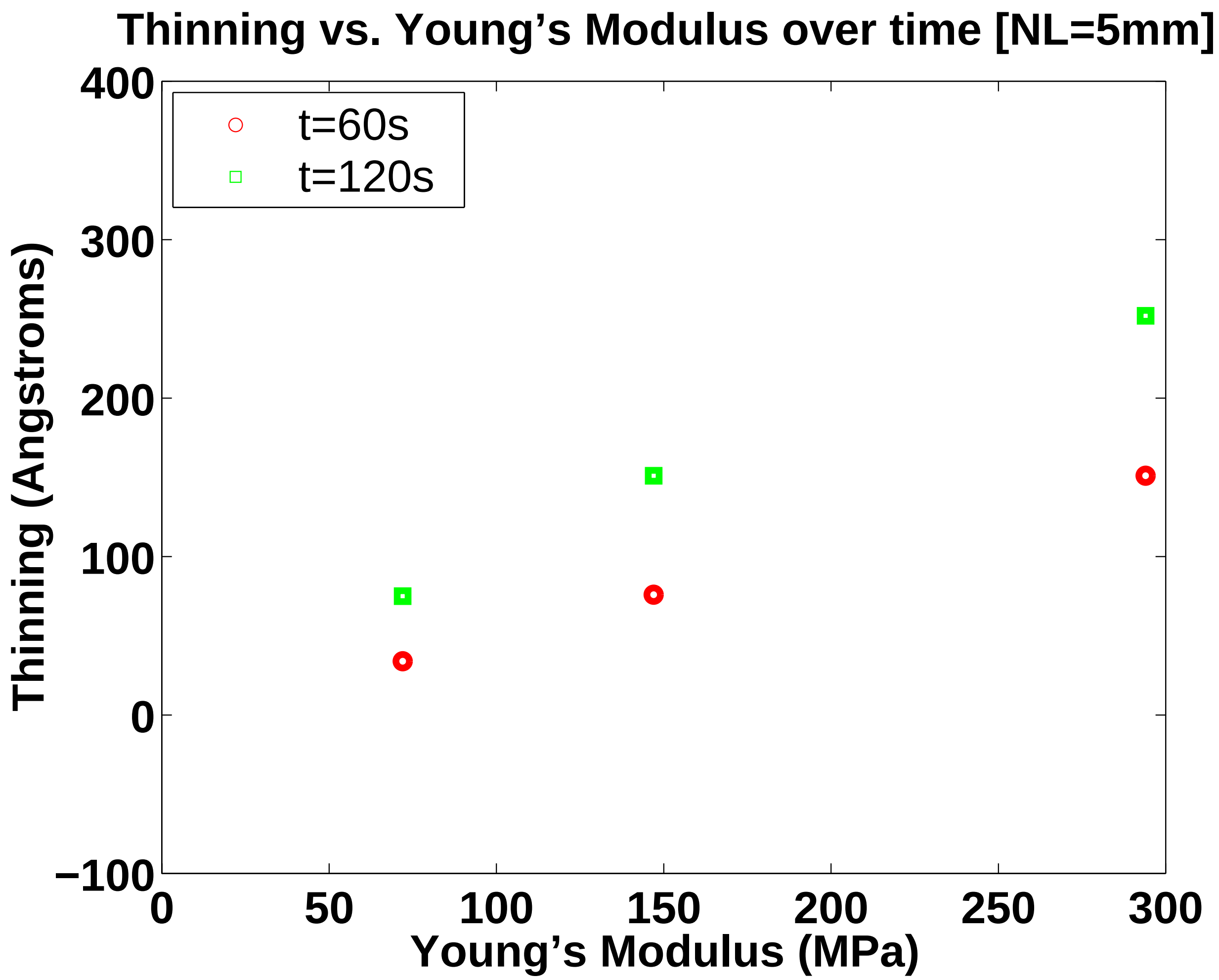
Model Analysis Results (I)



Model Analysis Results (II)



Model Analysis Results (III)



Observations

- Thinning increases with planarization length
- Thinning increases with Young's modulus of pad
- Thinning increases with time

- ***Question: Can we confirm this observation experimentally?***

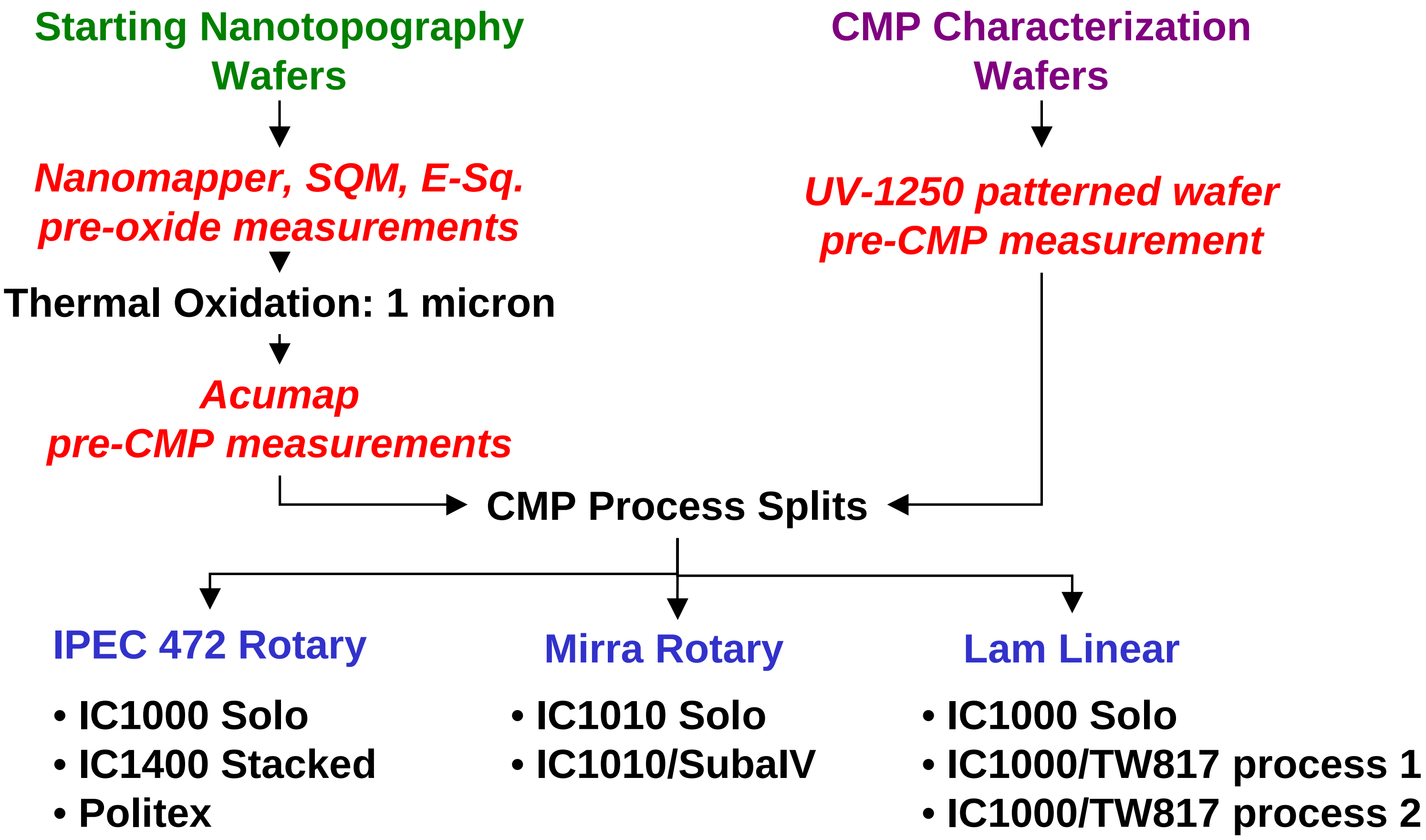
- ***Question: How does the thinning effect impact a shallow trench isolation process?***

4. Nanotopography & CMP Experiments

Experimental Approach

- Key Idea:
    - Use wafers with variety of nanotopography lengths
    - Polish wafers using processes with variety of planarization lengths
    - Measure BOTH planarization length AND wafer results
- Comparison to Previous Experiments
    - Xu et al. (ESSL '98): showed CMP oxide thinning related to both original wafer height variations and pad properties
    - JEIDA experiments: splits on wafers and CMP pads, but no measurement of planarization length
- MIT/ADE Experiment Goals:
    - Verify nanotopography length vs. planarization length hypothesis
    - Provide a quantitative and predictive model for the impact of starting wafer nanotopography for any characterized CMP process

Process and Measurements



Starting Nanotopography Wafers

Nanomapper, SQM, E-Sq. pre-oxide measurements

Thermal Oxidation: 1 micron

Acumap pre-CMP measurements

CMP Characterization Wafers

UV-1250 patterned wafer pre-CMP measurement

CMP Process Splits

IPEC 472 Rotary

- IC1000 Solo
- IC1400 Stacked
- Politex

Mirra Rotary

- IC1010 Solo
- IC1010/SubaIV

Lam Linear

- IC1000 Solo
- IC1000/TW817 process 1
- IC1000/TW817 process 2

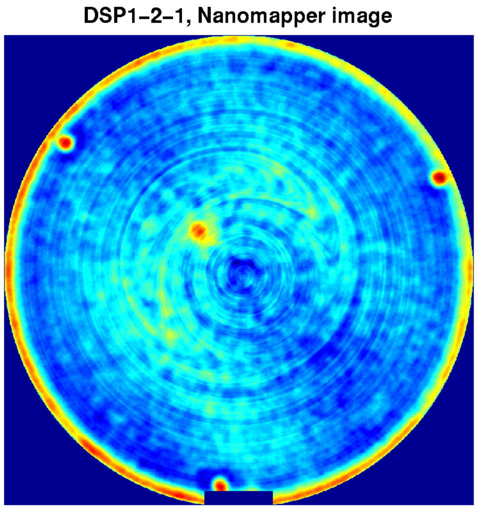
Acumap post-CMP measurements
$\Rightarrow$ *oxide thinning*

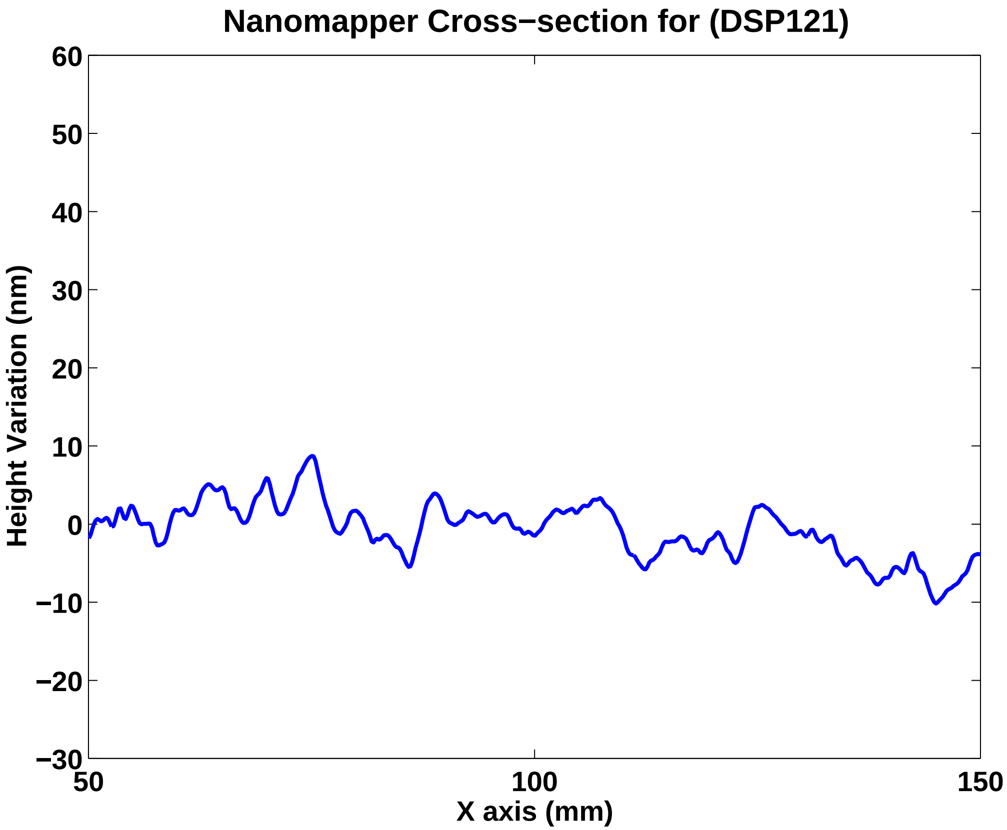
UV-1250 patterned wafer post-CMP measurements
$\Rightarrow$ *planarization length*

Starting Nanotopography Wafers

- Select lots of epi wafers fabricated with different starting wafer preparation recipes to generate a range of nanotopography features
  - Double-sided polish (DSP)
  - Single-sided polish (SSP)
  - Different **length scales** and **surface characteristics**
- Wafer characteristics:
  - DSP1 (47 wafers): small amplitude, medium length
  - DSP2 (10 wafers): doping striations
  - SSP1 (60 wafers): ring-like variation, long length
  - SSP2 (50 wafers): clusters or "blotches" at shorter length
  - SSP3 (50 wafers): blotches at longer length

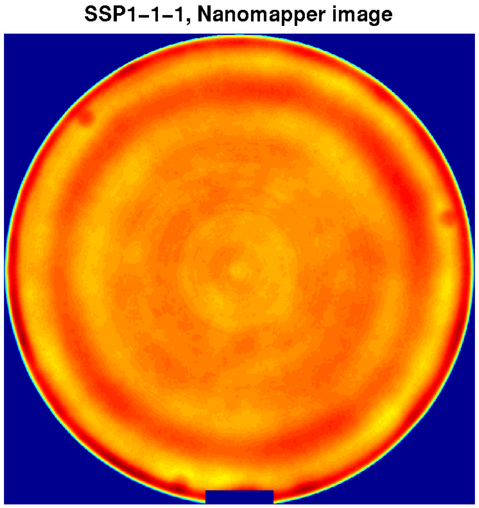
Double-Sided Polish Wafer (DSP1)

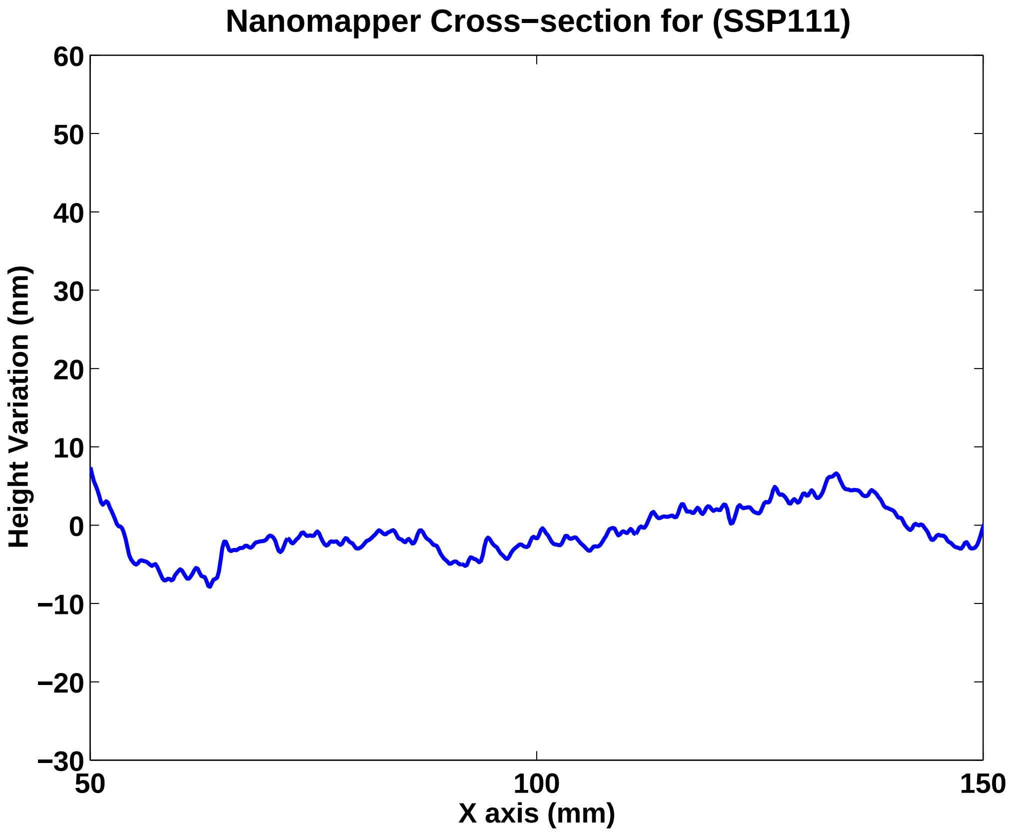




- ~ 10 nm height variations
- short wavelength

Single-Sided Polish Wafer (SSP1)

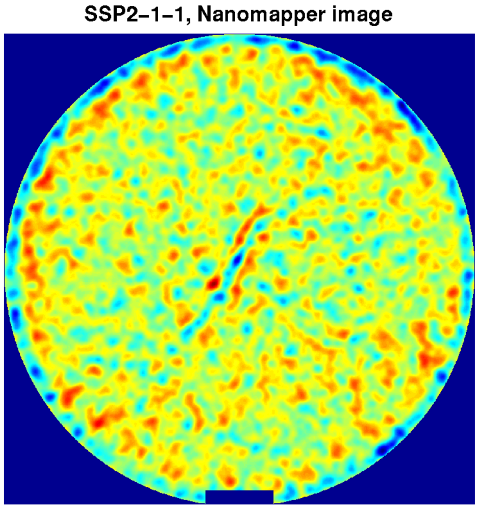


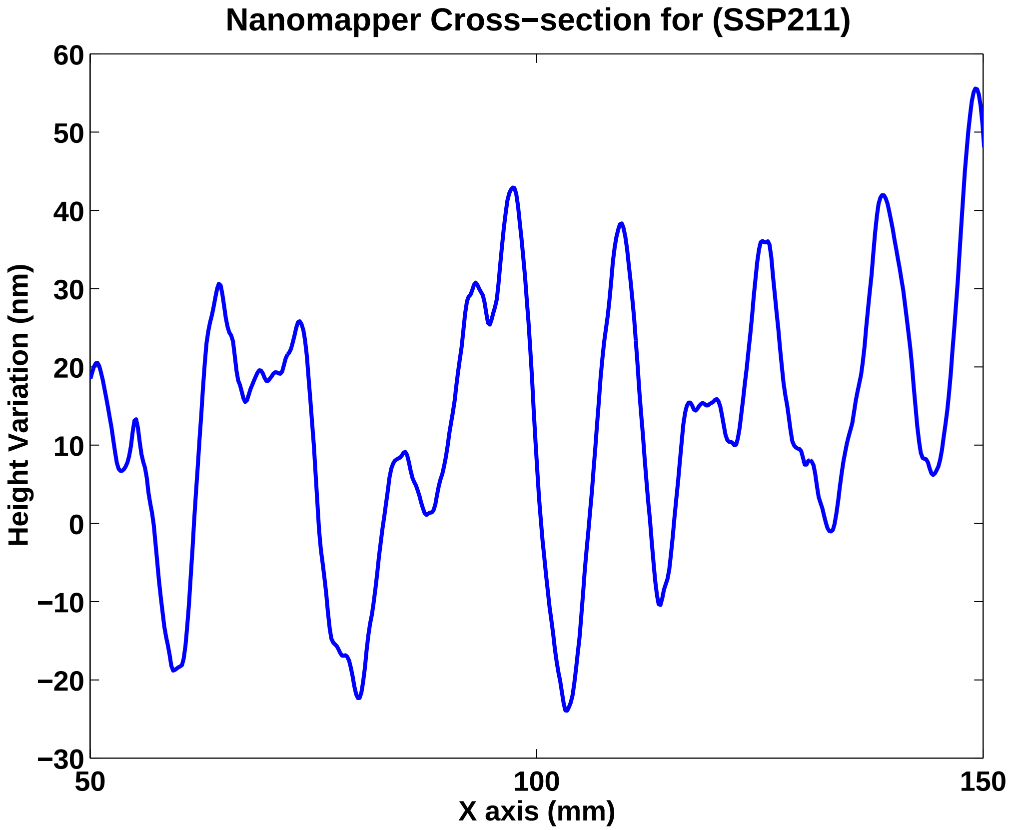


- ~ 20 nm height variations
- very long wavelength (w/ noise)

NanoMapper™

Single-Sided Polish Wafer (SSP2)

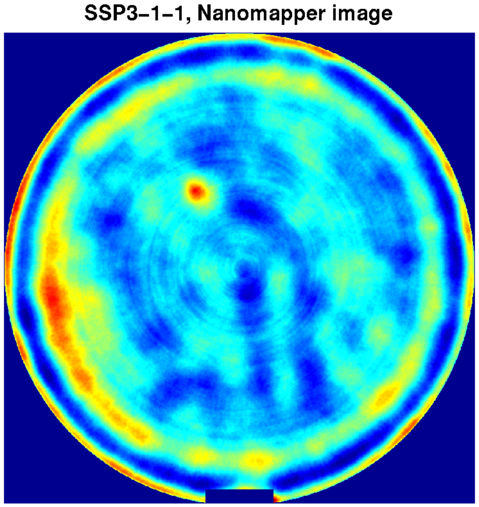


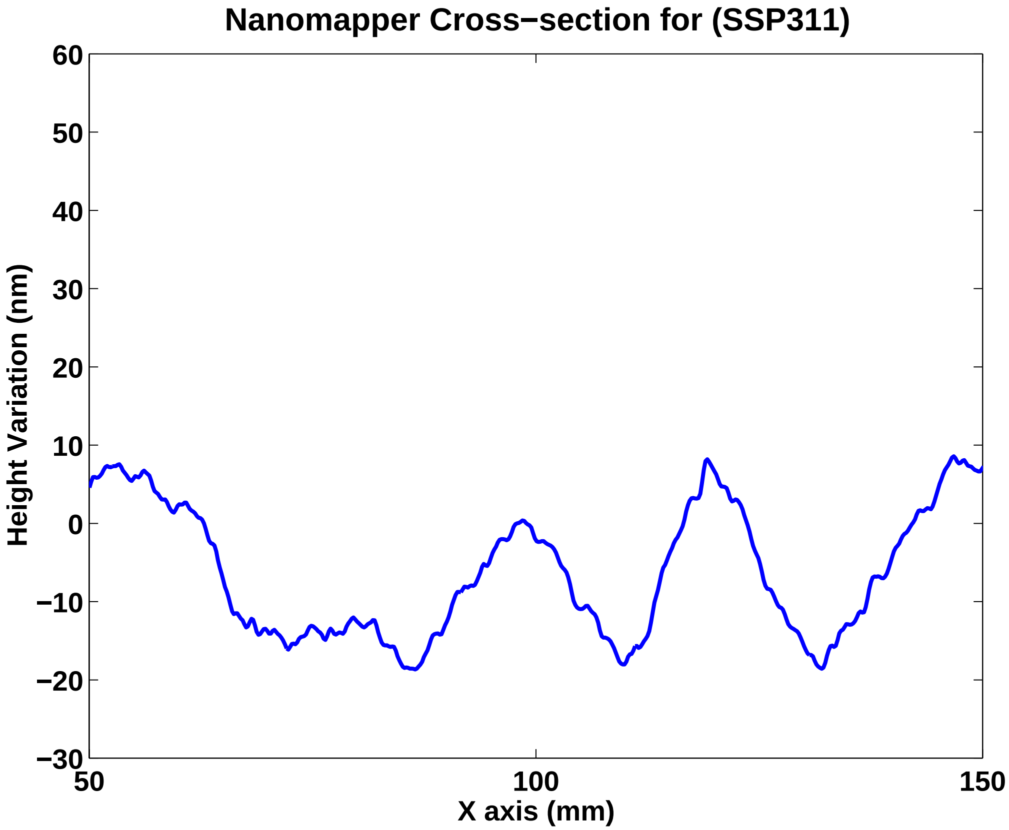


- ~ 50 nm height variations
- short wavelength

NanoMapper™

Single-Sided Polish Wafer (SSP3)





- ~ 30 nm height variations
- long wavelength

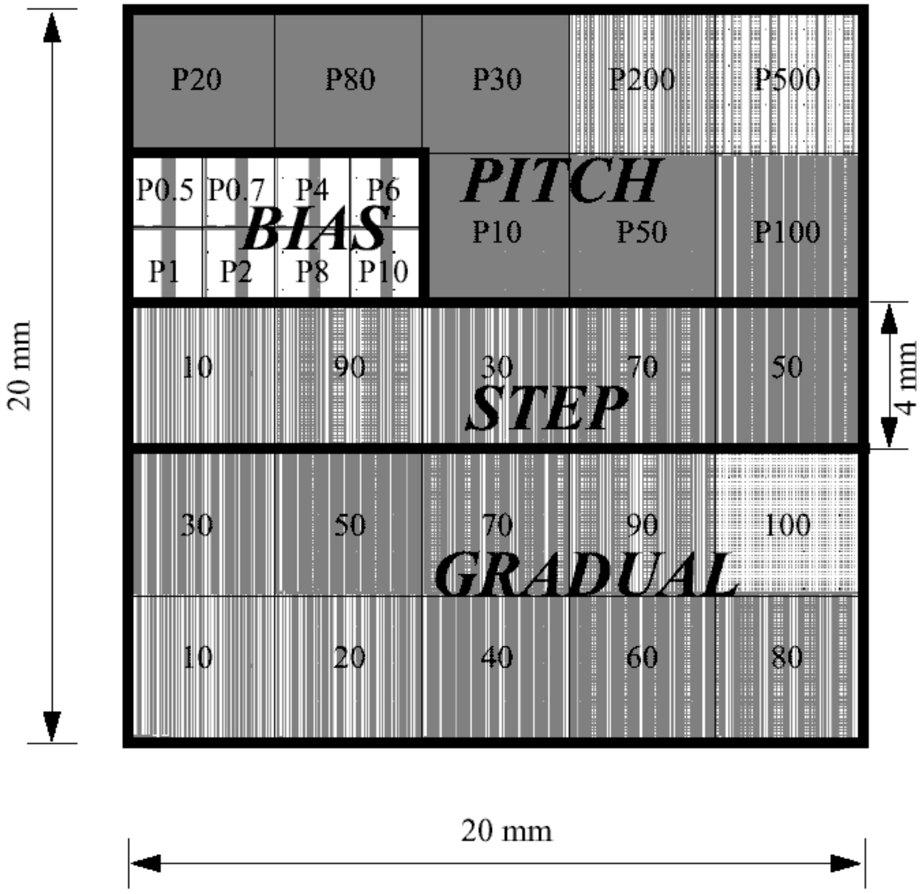
CMP Process/Pad Splits

- Planarization length depends on:
  - **pad** (pad type, pad stack, pad thicknesses, grooving, ...)
  - process (slurry, pressure, weak function of velocity)
  - tool? (dependency on head, table, tool configuration unclear)
- Approach: use pad as dominant factor, and measure
  - pad/process/tool to generate planarization length splits
  - **measure** planarization for any given CMP pad/process/tool
- Pad and Estimated (Expected) Planarization Length Ranges:
  - IC1000 solo: 7-10 mm
  - IC1400 (IC1000/SubaIV) stacked: 3-7 mm
  - Politex: < 1 mm

Fab Sequence – Per Process Split

<table>
<tr><th colspan="7">sette ID:</th></tr>
<tr><th>sette Slot/ Run #</th><th>Wafer ID</th><th>CODE*</th><th>Wafer Type</th><th>Polish Time, sec</th><th>Pre-polish Thickness, um</th><th>Post-polish Thickness, um</th></tr>
<tr><td></td><td></td><td>D1</td><td>Dummy</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>D2</td><td>Dummy</td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>D3</td><td>Dummy</td><td></td><td></td><td></td></tr>
<tr><td>1</td><td></td><td>B1</td><td>Blanket Rate</td><td></td><td></td><td></td></tr>
<tr><td>2</td><td></td><td>B2</td><td>Blanket Rate</td><td></td><td></td><td></td></tr>
<tr><td colspan="7">Measure Blanket Wafers (see step instructions)</td></tr>
<tr><td>3</td><td></td><td>W1</td><td>DSP</td><td></td><td></td><td></td></tr>
<tr><td>4</td><td></td><td>W4</td><td>SSP1</td><td></td><td></td><td></td></tr>
<tr><td>5</td><td></td><td>W7</td><td>SSP2</td><td></td><td></td><td></td></tr>
<tr><td>6</td><td></td><td>B3</td><td>Blanket Rate</td><td></td><td></td><td></td></tr>
<tr><td>7</td><td></td><td>W10</td><td>SSP3</td><td></td><td></td><td></td></tr>
<tr><td>8</td><td></td><td>W2</td><td>DSP</td><td></td><td></td><td></td></tr>
<tr><td>9</td><td></td><td>W5</td><td>SSP1</td><td></td><td></td><td></td></tr>
<tr><td>10</td><td></td><td>P1</td><td>Patterned</td><td></td><td></td><td></td></tr>
<tr><td>11</td><td></td><td>B4</td><td>Blanket Rate</td><td></td><td></td><td></td></tr>
<tr><td>12</td><td></td><td>W8</td><td>SSP2</td><td></td><td></td><td></td></tr>
<tr><td>13</td><td></td><td>W11</td><td>SSP3</td><td></td><td></td><td></td></tr>
<tr><td>14</td><td></td><td>W3</td><td>DSP</td><td></td><td></td><td></td></tr>
<tr><td>15</td><td></td><td>C2</td><td>Patterned</td><td></td><td></td><td></td></tr>
<tr><td>16</td><td></td><td>B5</td><td>Blanket Rate</td><td></td><td></td><td></td></tr>
<tr><td>17</td><td></td><td>W6</td><td>SSP1</td><td></td><td></td><td></td></tr>
<tr><td>18</td><td></td><td>W9</td><td>SSP2</td><td></td><td></td><td></td></tr>
<tr><td>19</td><td></td><td>W12</td><td>SSP3</td><td></td><td></td><td></td></tr>
<tr><td>20</td><td></td><td>W13</td><td>SSP4</td><td></td><td></td><td></td></tr>
<tr><td>21</td><td></td><td>B6</td><td>Blanket Rate</td><td></td><td></td><td></td></tr>
</table>

MIT CMP Characterization Wafers - Planarization Length Measurement



- Wafers patterned with lines and spaces to generate different regions:
  - **step and gradual density**
    - 10% to 100% raised area
  - **pitch regions**
    - 50% density, vary line/space
- Measurement of up and down areas enables extraction of:
  - **planarization length**
  - **step height dependencies**

Planarization Length – Extracted Results

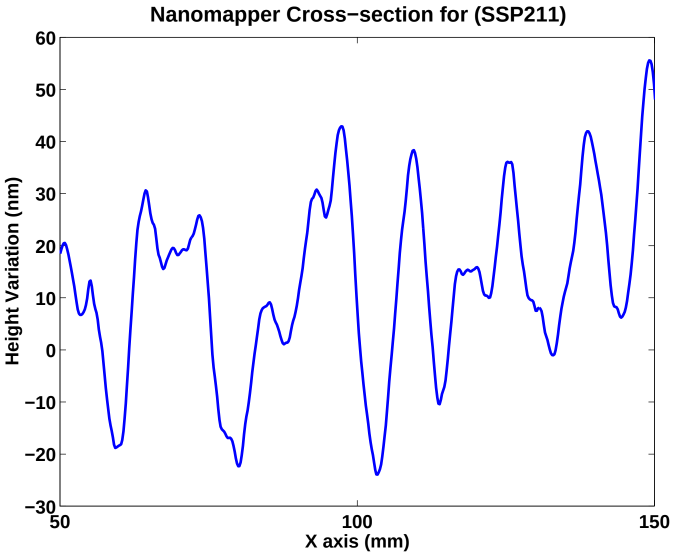
Pad/Process Split	Planarization Length
Politex	1.9 mm
IC1400/Stacked	3.4 mm
IC1010/Stacked	6.5 mm
IC1000/Solo	8.5 mm
IC1010/Solo	9.7 mm

- Three additional pad/process splits still being measured/analyzed

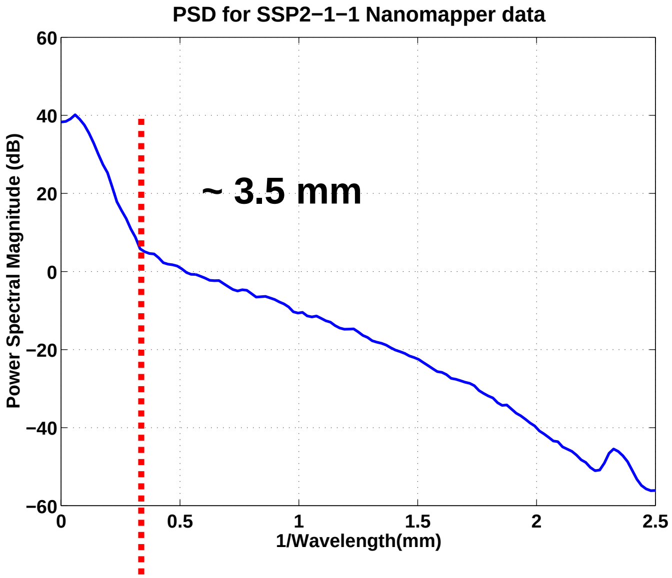
Analysis and Modeling

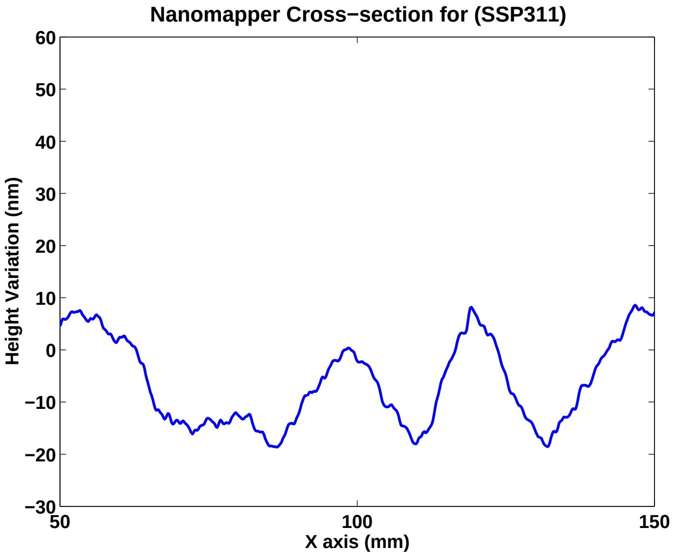
1. CMP Process Characterization – Planarization Length
   - Extract for each process split using patterned wafer data
2. Starting Wafer Characterization – Nanotopography Length
   - Need definition: power spectral density or other metric
3. Nanotopography and CMP Thinning Correlations
   - Graphical (qualitative) correlations by images
   - Calculate 2D nanotopography vs. oxide-thickness correlation coefficient
   - Test PL vs. NL length hypothesis
4. Evaluate different candidate CMP models (future work)
   - Using pre-CMP data and extracted planarization length
     - predict post-CMP oxide thickness using CMP model
     - compare to measured post-CMP oxide thickness
5. Evaluate different nanotopography metrics and specs (future)

Nanotopography Length – PSD Approach

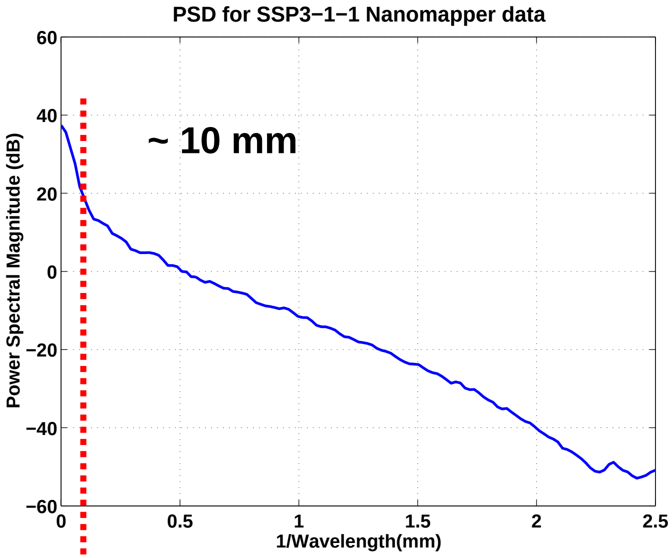


SSP2 Wafer





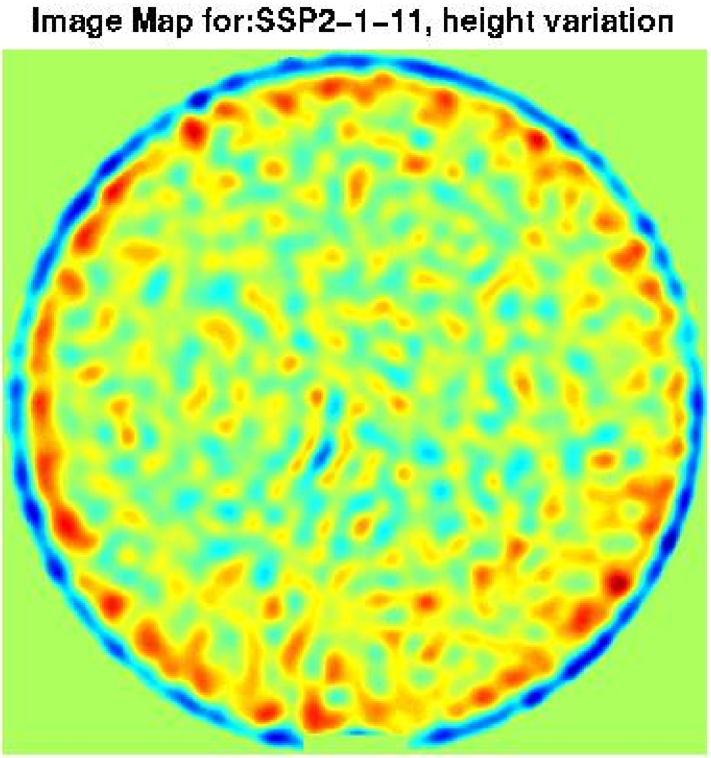
SSP3 Wafer



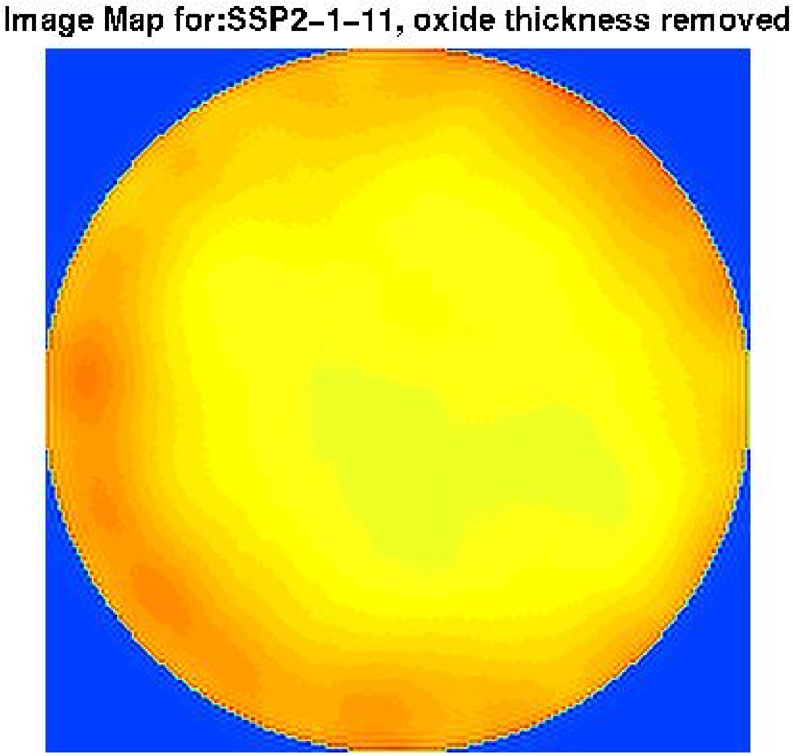
5. Experimental Results

Case 1: Short NL & Short PL (Soft Pad)

- **SSP2 wafer; Politex pad/process with PL = 1.9 mm**



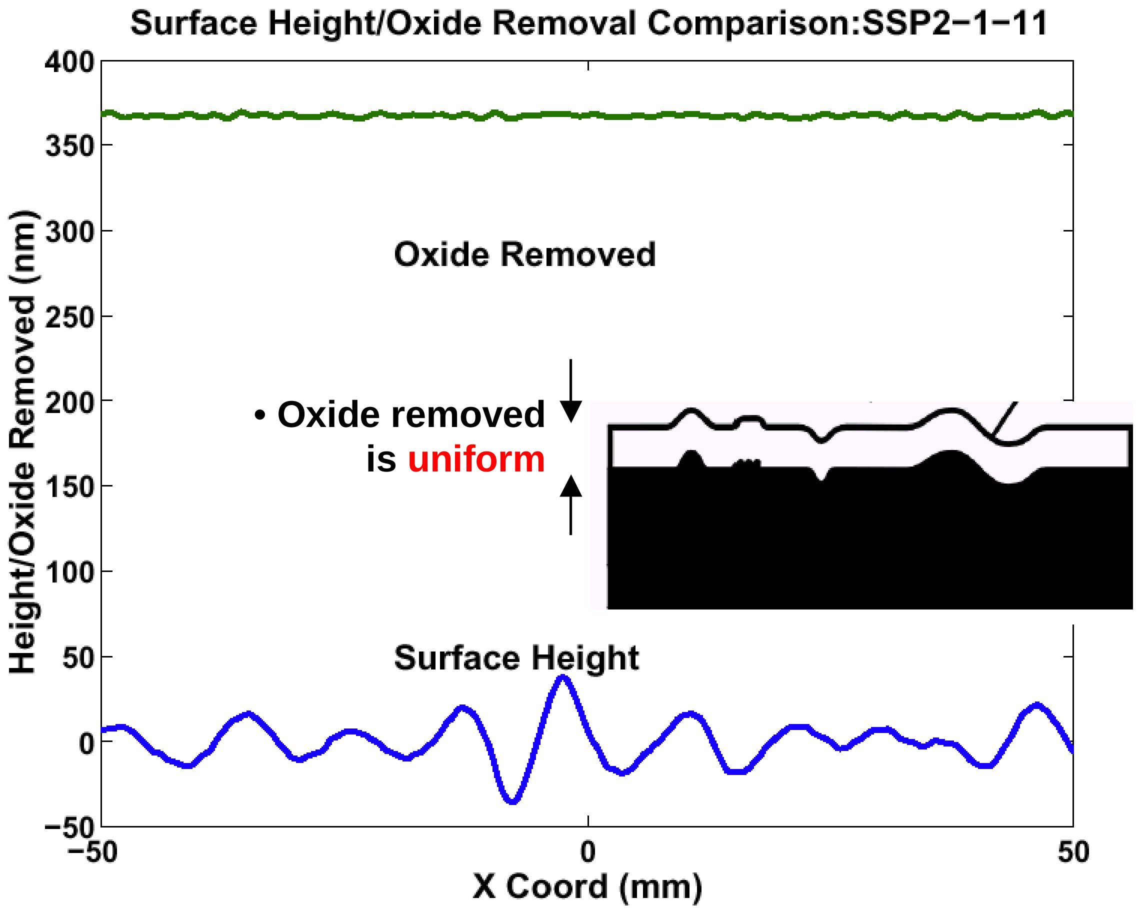
- **Starting nanotopography for SSP2 Wafer**



- **Oxide removed with Politex pad**

⇒ wafer level CMP removal nonuniformity is observed

Case 1: Short NL & Short PL (Soft Pad)



- Oxide removed is uniform

Split Details

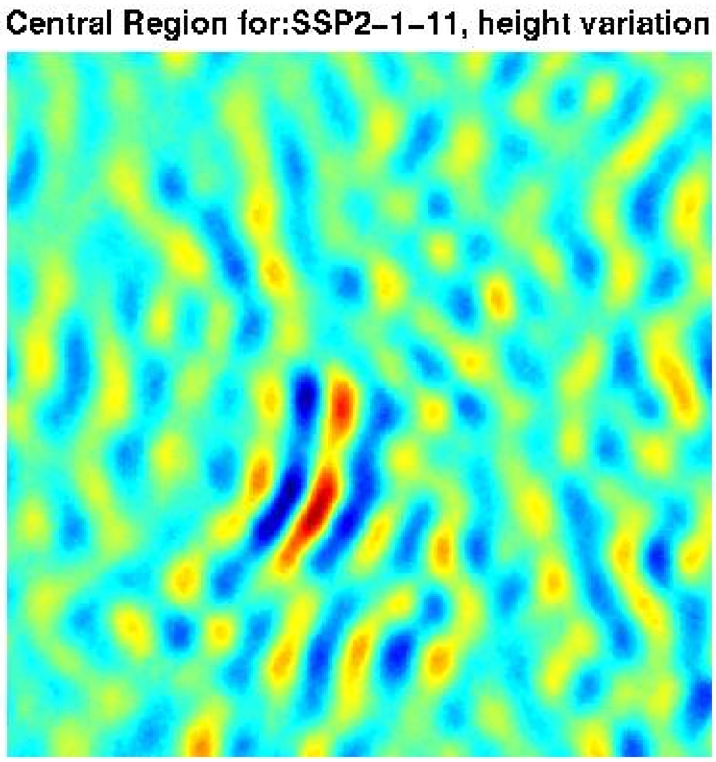
- Politex pad
  (1.9mm planarization length)
- SSP2 wafer
  (short-range nanotopography)

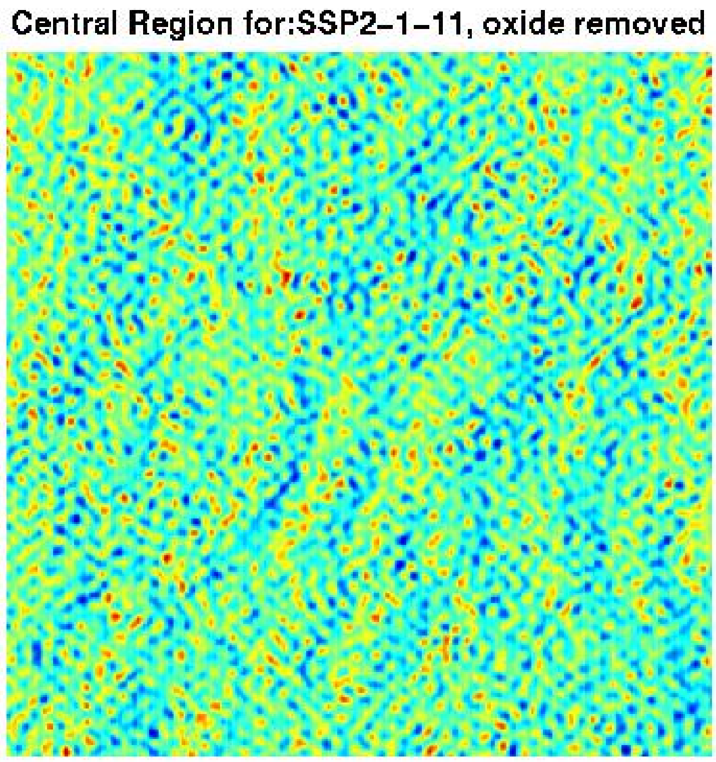
Result

- Nanotopography *not* transmitted into surface oxide film
- Filtered data used to remove wafer scale oxide removal non-uniformity

Case 1: Short NL & Short PL (Soft Pad)

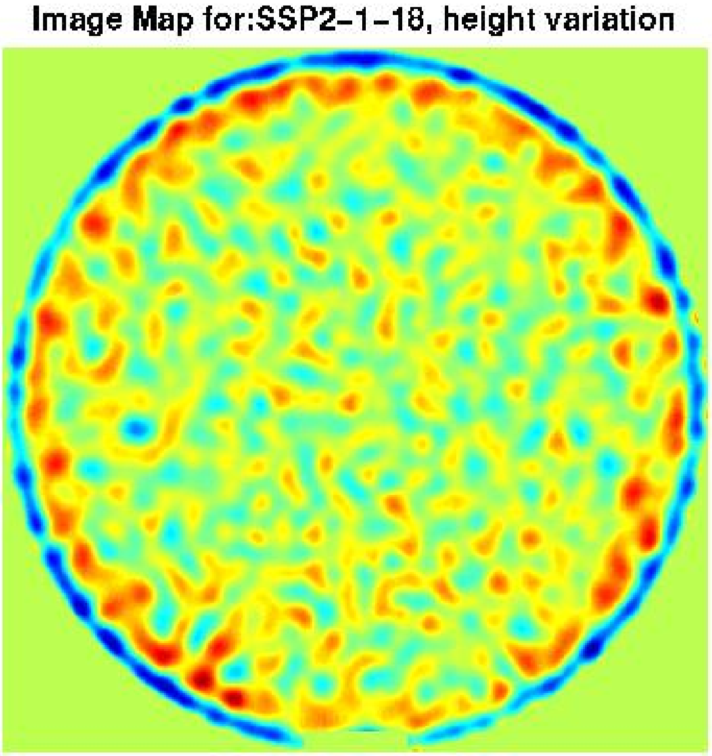
- SSP2 wafer; Politex pad, process has PL = 1.9 mm
- Variation for central 100mm portion of wafer
  - Deviation in each normalized: full range variation around each mean shown



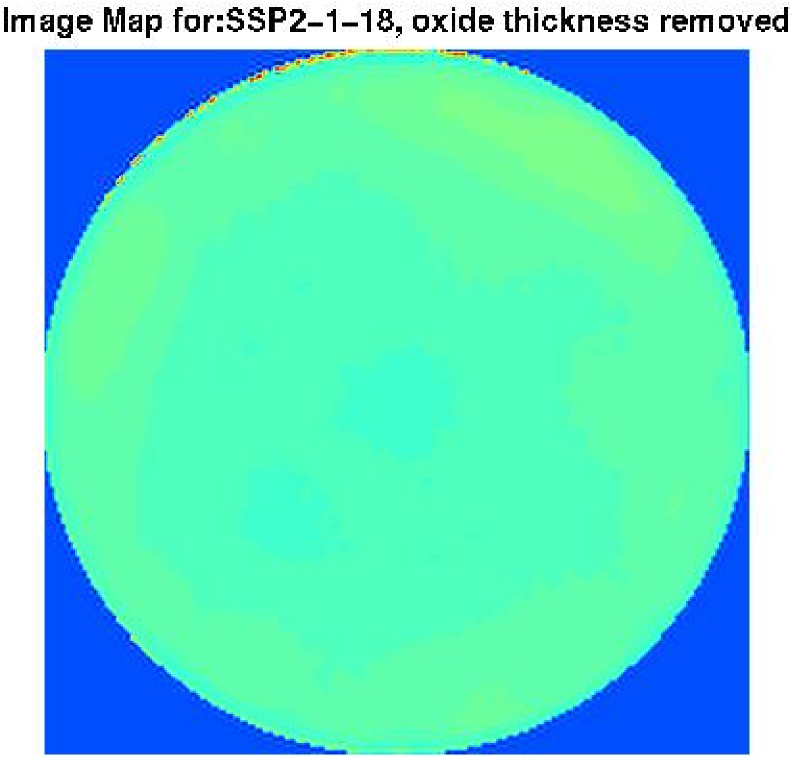


Case 2: Short NL & Medium PL (Stack Pad)

- SSP2 wafer; IC1400 stacked pad/process with PL = 3.4 mm



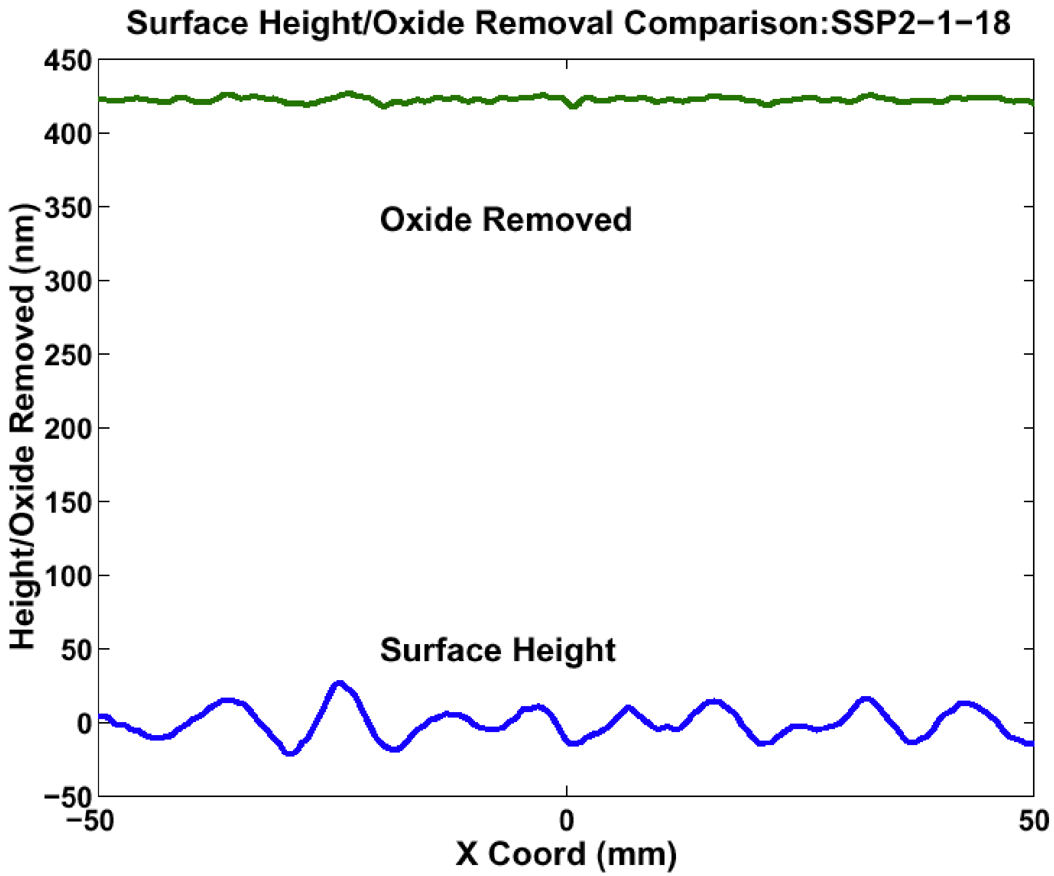
- Starting nanotopography for SSP2 Wafer



- Oxide removed with IC1400 stacked pad

⇒ slight nanotopography is superimposed on wafer level CMP nonuniformity

Case 2: Short NL & Medium PL (Stack Pad)



Split Details

- IC1400 stacked pad (3.4mm planarization length)
- SSP2 wafer (short-range nanotopography)

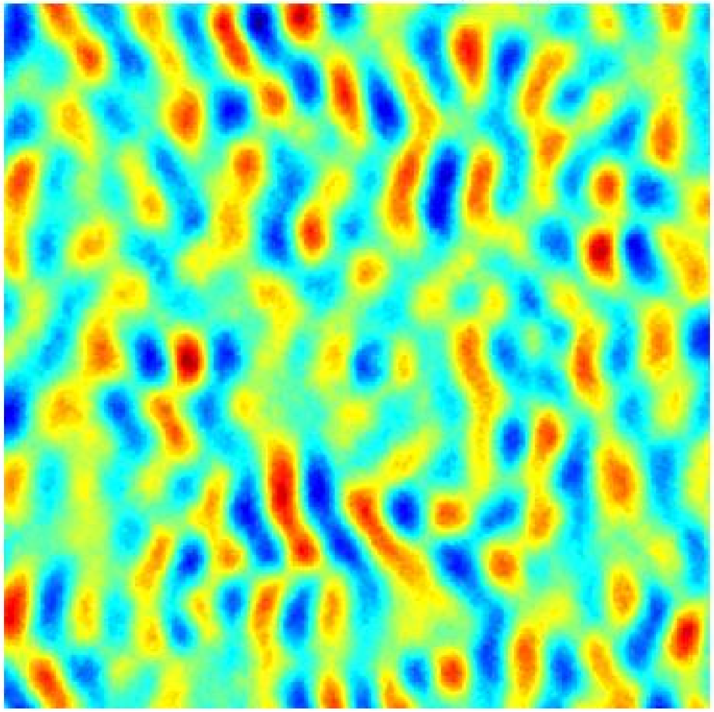
Result

- Only limited nanotopography propagation into oxide film
- Filtered data used (removes wafer scale polish non-uniformity)

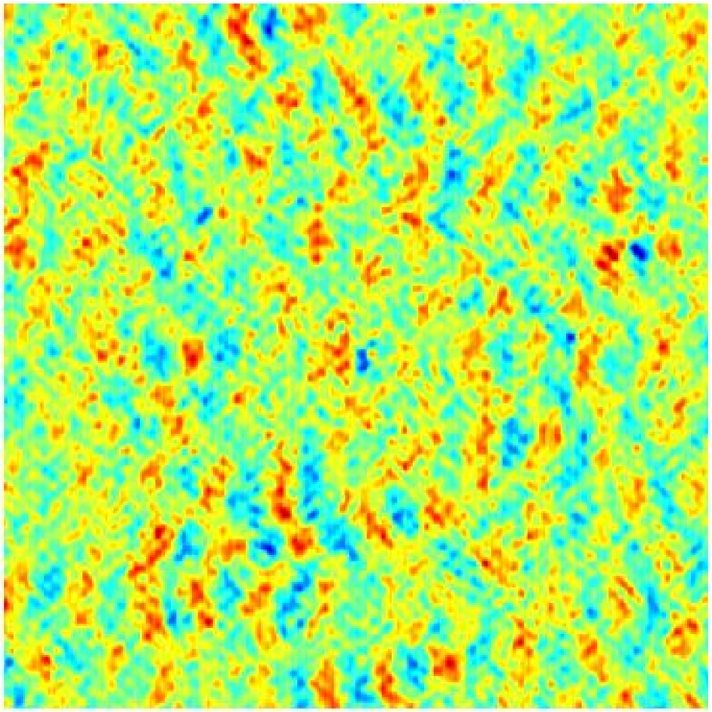
Case 2: Short NL & Medium PL (Stack Pad)

- SSP2 wafer; IC1400 stacked pad, process has PL = 3.4 mm
- Variation for central 100mm portion of wafer
  - Deviation in each normalized: full range variation around each mean shown

Central Region for:SSP2-1-18, height variation

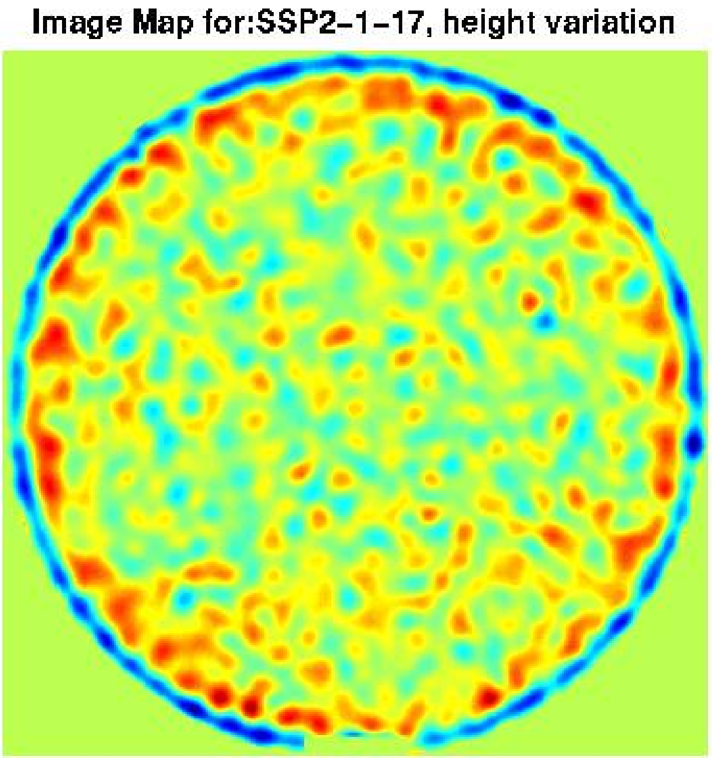


Central Region for:SSP2-1-18, oxide removed

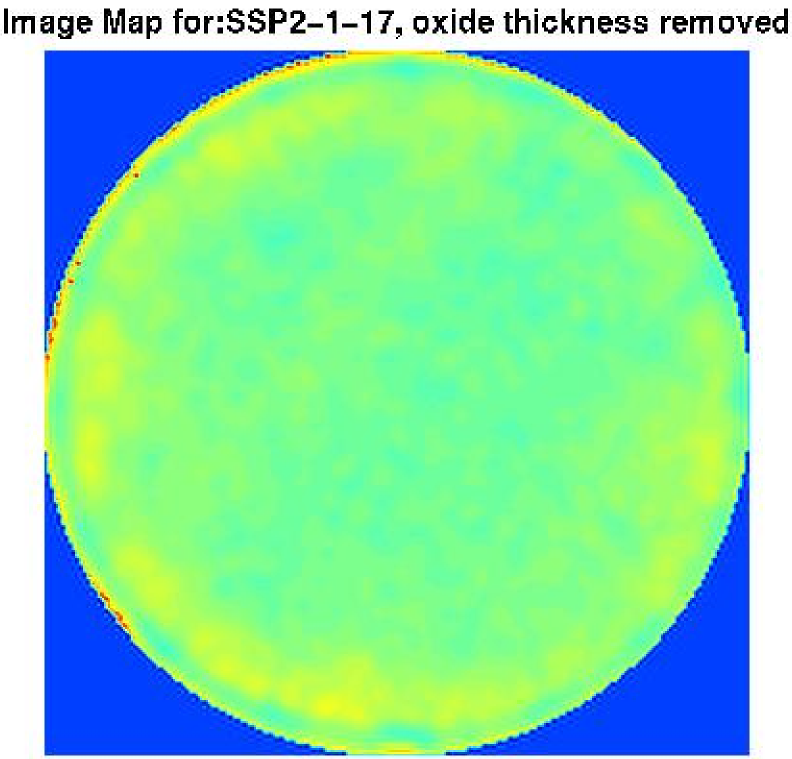


Case 3: Short NL & Long PL (Stiff Pad)

- **SSP2 wafer; IC1000 solo pad/process with PL = 8.5 mm**



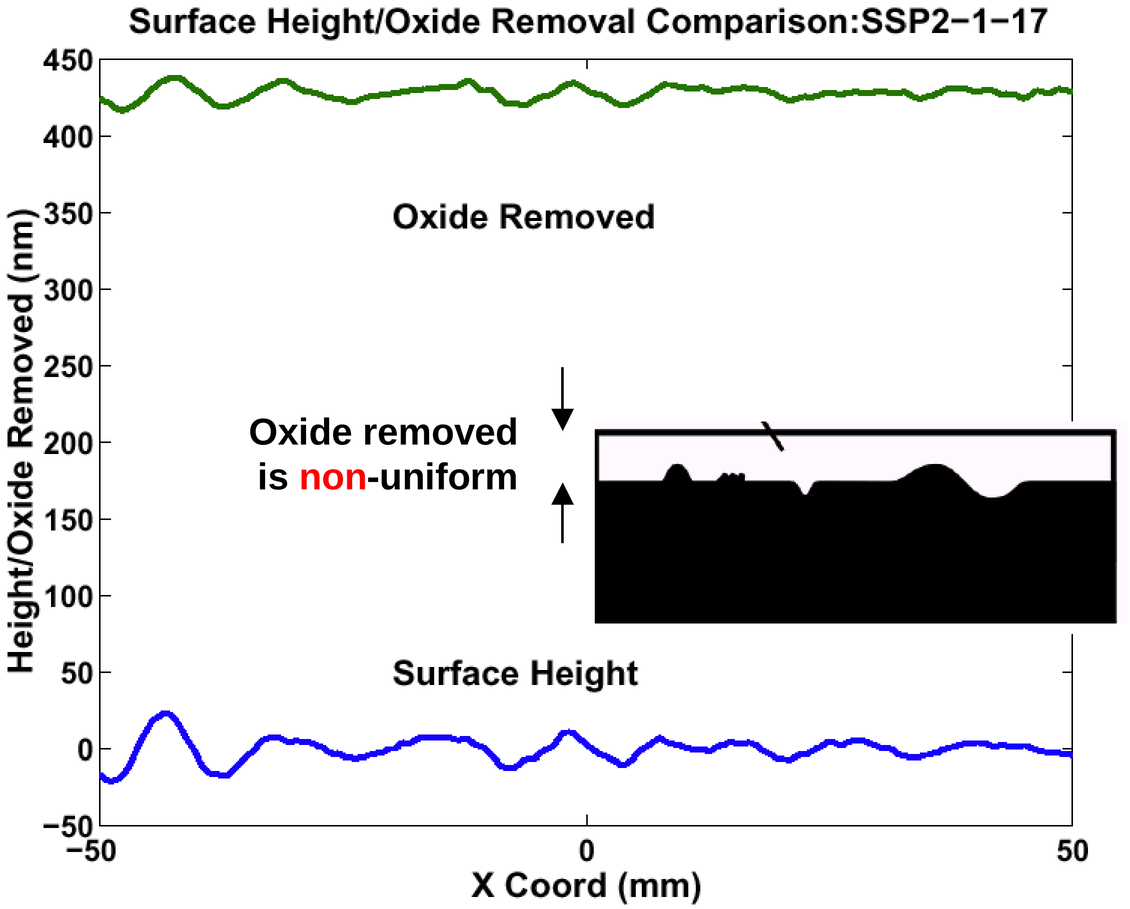
- **Starting nanotopography for SSP2 Wafer**



- **Oxide removed with IC1000 solo pad**

⇒ nanotopography is superimposed on wafer level CMP nonuniformity

Case 3: Short NL & Long PL (Stiff Pad)



Split Details

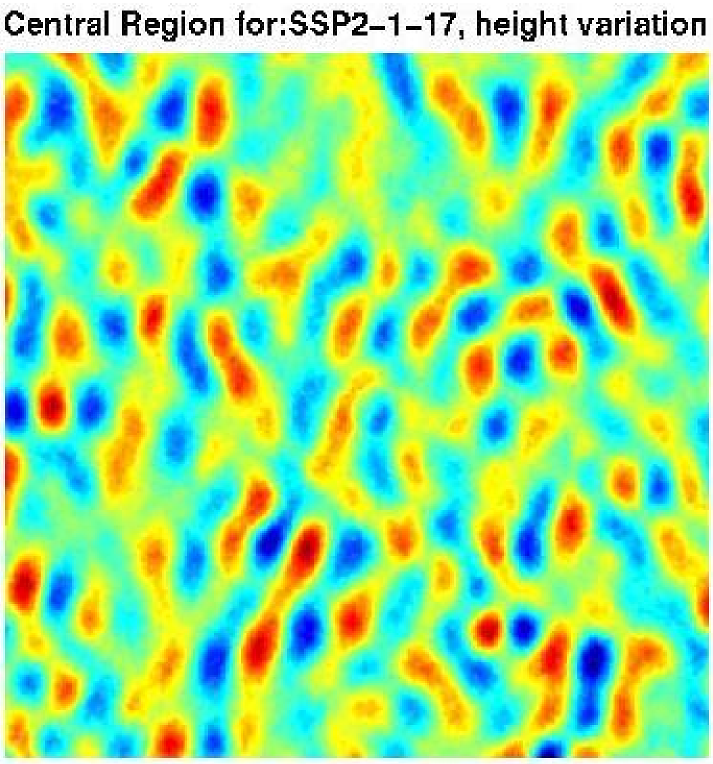
- IC1000 solo pad
  (8.5mm planarization length)
- SSP2 wafer
  (short-range nanotopography)

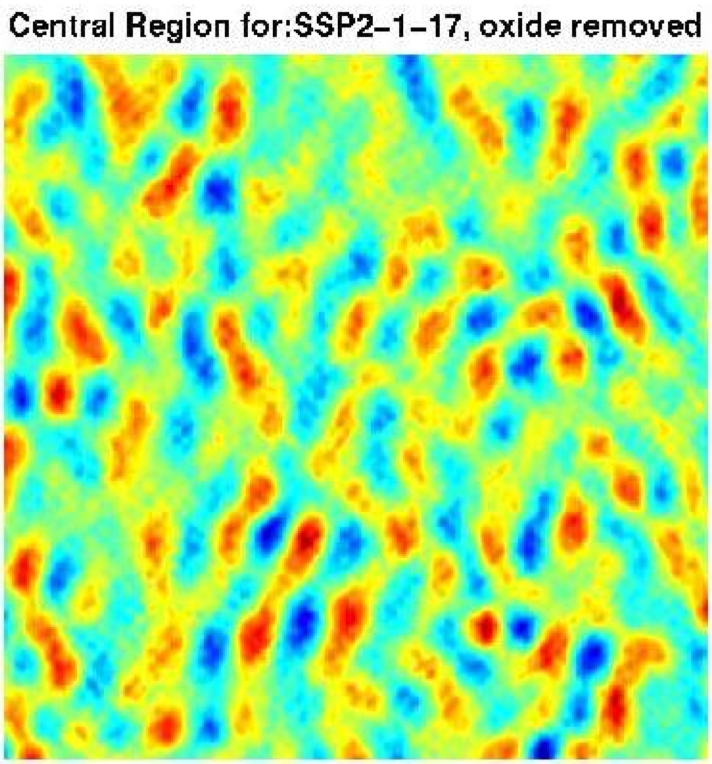
Result

- Nanotopography *propagates* strongly into oxide film
- Filtered data used (removes wafer scale polish non-uniformity)

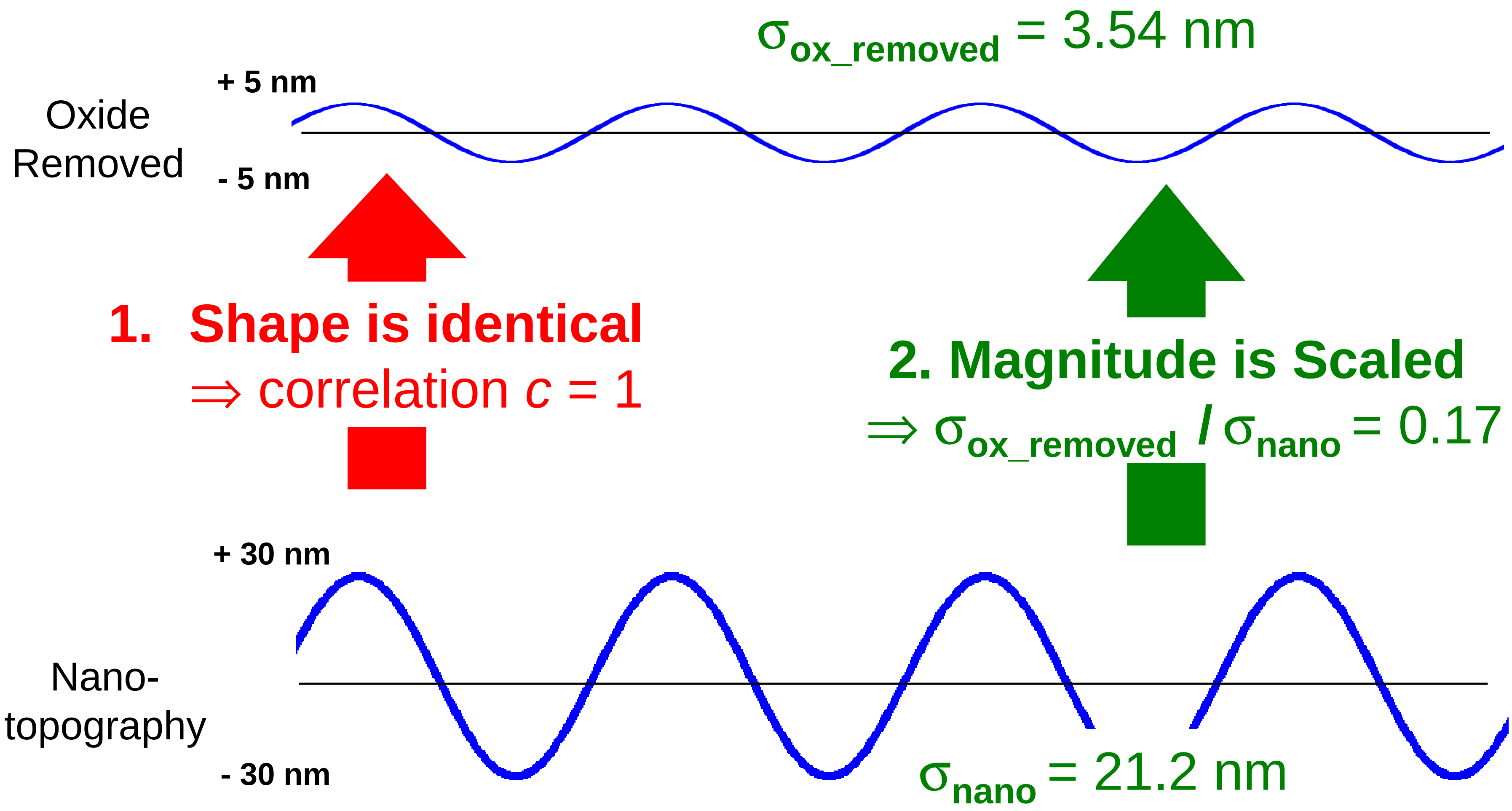
Case 3: Short NL & Long PL (Stiff Pad)

- SSP2 wafer; IC1000 solo pad, process has PL = 8.5 mm
- Variation for central 100mm portion of wafer
  - Deviation in each normalized: full range variation around each mean shown


Central Region for:SSP2-1-17, height variation


Central Region for:SSP2-1-17, oxide removed

Propagation of Nanotopography to Oxide During CMP – Correlation and Std. Dev.



$\sigma_{ox\_removed} = 3.54$ nm

1. **Shape is identical**
   $\Rightarrow$ correlation $c = 1$

2. **Magnitude is Scaled**
   $\Rightarrow \sigma_{ox\_removed} / \sigma_{nano} = 0.17$

$\sigma_{nano} = 21.2$ nm

Correlation Between Nanotopography Height Variation and Oxide Removed in CMP

- Calculate a correlation coefficient *c* over 2D map *(i,j)* to capture "similarity" in the ***shape of the variation*** (% deviations around each mean) between:
  - *x:* nanotopography height
  - *y*: oxide removed:

$$c = \frac{\sum_i \sum_j \left(x_{ij} - \mu_x\right)\left(y_{ij} - \mu_y\right)}{\sigma_x \sigma_y}$$

- $c \to 0$: no correlation

  $c \to 1$: complete (positive) correlation

  $c \to -1$: complete correlation (inversion)

- Calculate the standard deviation σ_x and σ_y to summarize the ***magnitude of the variation*** in the nanotopography and the polished oxide thickness, respectively

Nanotopography – Oxide: Correlations

NL > PL

NL < PL

Nanotopography Wafer Type	transmitted shape: corr. coef. ***c***				
SSP1 long spatial λ	0.07	0.10	0.42	0.37	0.77
SSP3	0.10	0.28	0.53	0.38	0.69
DSP1	0.07	0.22	0.65	0.31	0.73
SSP2 short spatial λ	0.38	0.72	0.72	0.84	0.79
	1.9 mm	3.4 mm	6.4 mm	8.4 mm	9.7 mm
	Politex	IC1400	IC1010	IC1000 solo	IC1010 solo
	Planarization Length / Pad				

Filtered to remove wafer level trend

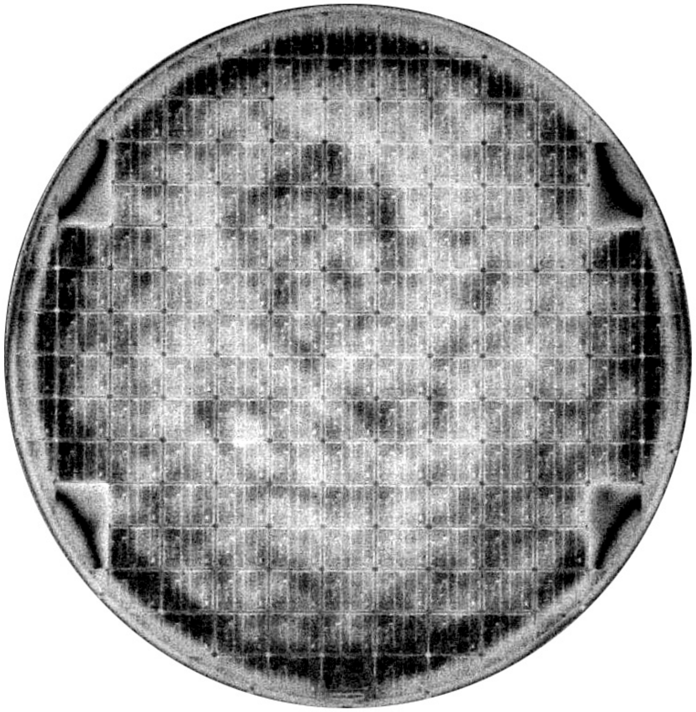
Nanotopography – Oxide: Std. Devs.

		transmitted height: $\sigma_{ox\_removed} / \sigma_{nano}$ $\sigma_{ox\_removed}$ **(nm) /** σ_{nano} **(nm)**				
Nanotopography Wafer Type	SSP1 long spatial λ	0.66 **0.91/1.38**	0.59 **0.82/1.40**	0.66 **0.86/1.31**	1.19 **1.54/1.29**	1.02 **1.28/1.26**
	SSP3	0.48 **0.86/1.79**	0.51 **0.92/1.81**	0.58 **1.05/1.81**	1.09 **1.90/1.74**	0.84 **1.48/1.76**
	DSP1	0.40 **0.88/2.19**	0.49 **1.19/2.43**	0.67 **1.41/2.10**	0.86 **2.09/2.44**	0.83 **1.78/2.15**
	SSP2 short spatial λ	0.10 **0.89/9.03**	0.17 **1.33/7.88**	0.37 **2.70/7.29**	0.62 **4.53/7.27**	0.76 **5.65/7.48**
		1.9 mm	3.4 mm	6.4 mm	8.4 mm	9.7 mm
		Politex	IC1400	IC1010	IC1000 solo	IC1010 solo
		Planarization Length / Pad				

Filtered to remove wafer level trend

6. Nanotopography Effect on Shallow Trench Isolation (STI) CMP

Example of Film Color Variation after STI Polishing



Film Color Variation after STI-CMP Direct Polishing

- Surface nanotopography could impact many sites
- Nanotopography features will be random in size and location
- Potential device performance degradation and yield loss in the related dies

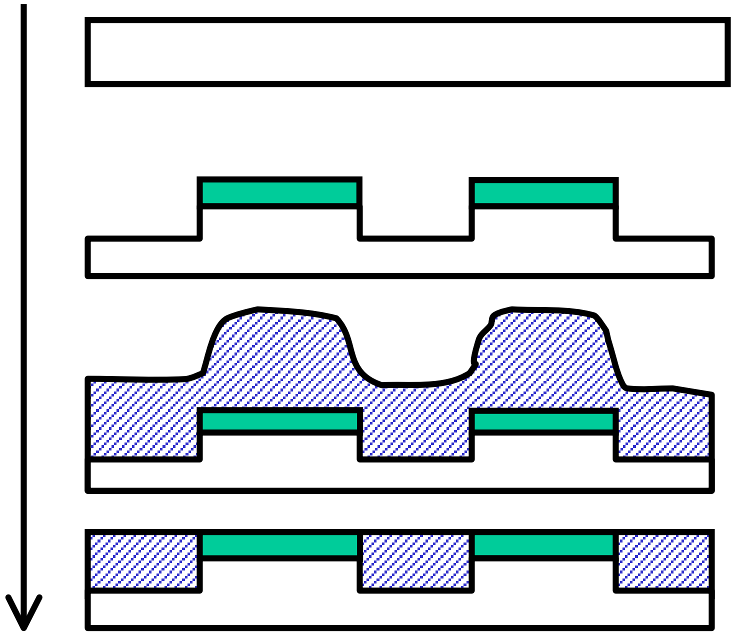
Xia et al., “Effect of Nanotopology on CMP,” 1999 Int. CMP Symposium

Nanotopography Impact on STI

- Nanotopography causes problems in the polishing of STI structures:
  - Difficult to clear oxide
  - Excessive nitride overpolishing
- There are many sources of variation in CMP. Nanotopography can create difficult problems compared to:
  - Wafer scale CMP polish rate nonuniformity
  - Die scale pattern dependencies

Shallow Trench Isolation (STI) Process Flow (Ideal Case)

- **Polished Starting Wafer**
- **Nitride/Oxide deposition, pattern, etch and trench etch**
- **Trench oxide deposition**
- **CMP of overburden oxide**



🟩 Nitride/Oxide Pad Stack

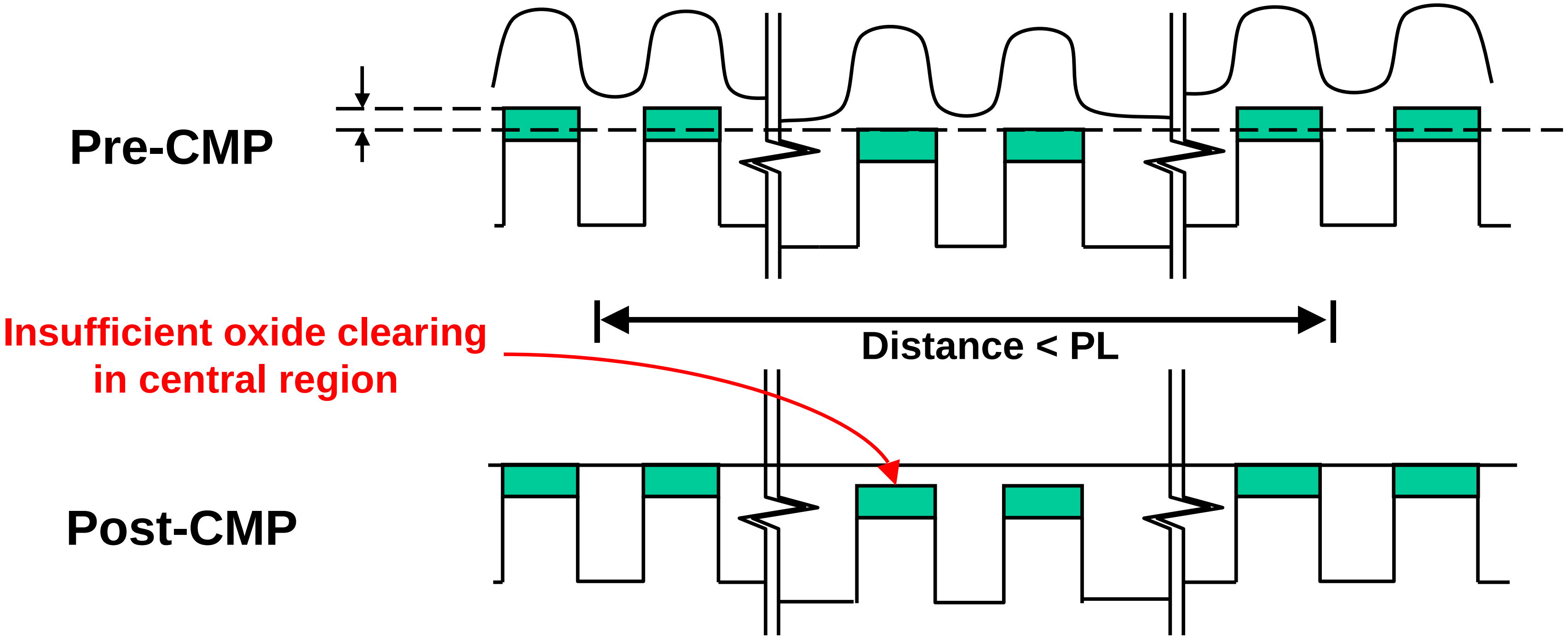
☐ Silicon Substrate

▨ Silicon Dioxide

Problem #1: Difficulty of Clearing

- Oxide polish intended to “stop” on nitride but *must* clear above *all* nitride structures (active areas) in order to yield
- Consider trench/active areas which are in a recessed region smaller than the planarization length due to nanotopography

⇒ CMP pad/process does not bend into region and fails to clear oxide



Pre-CMP

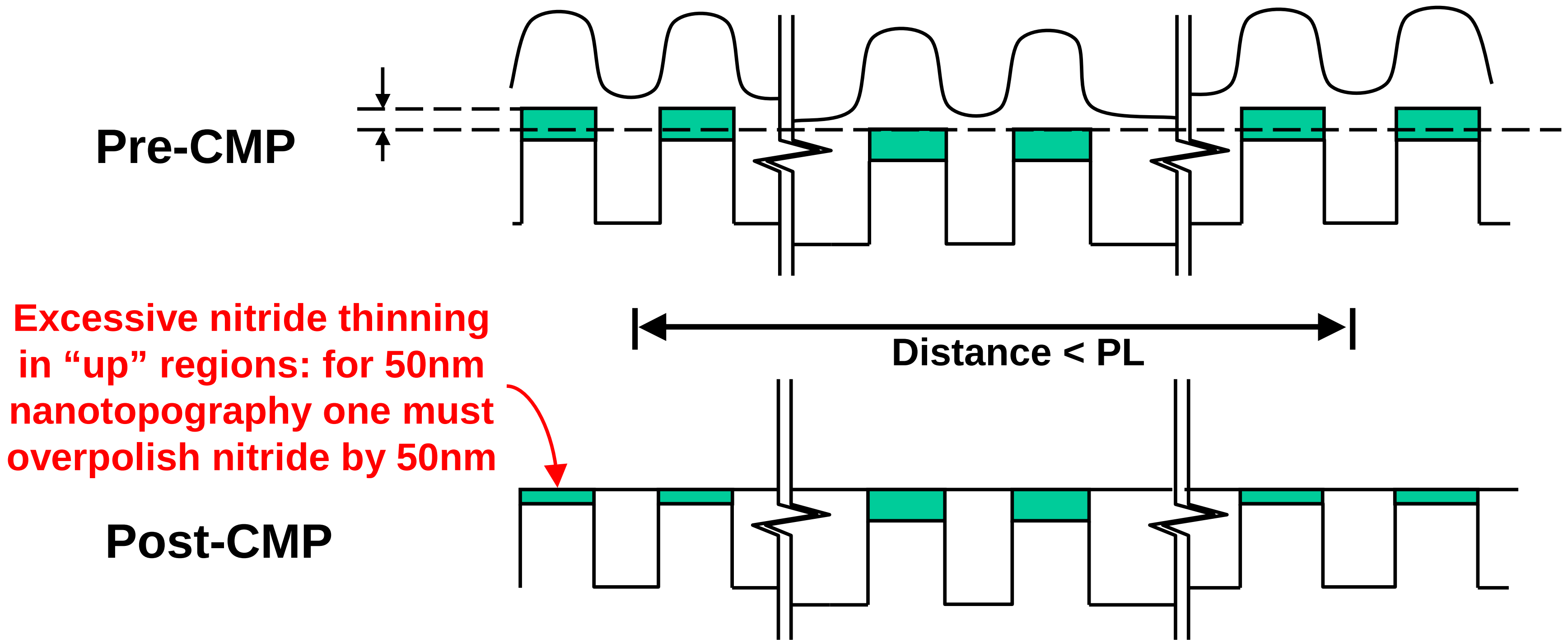
Insufficient oxide clearing in central region

Distance < PL

Post-CMP

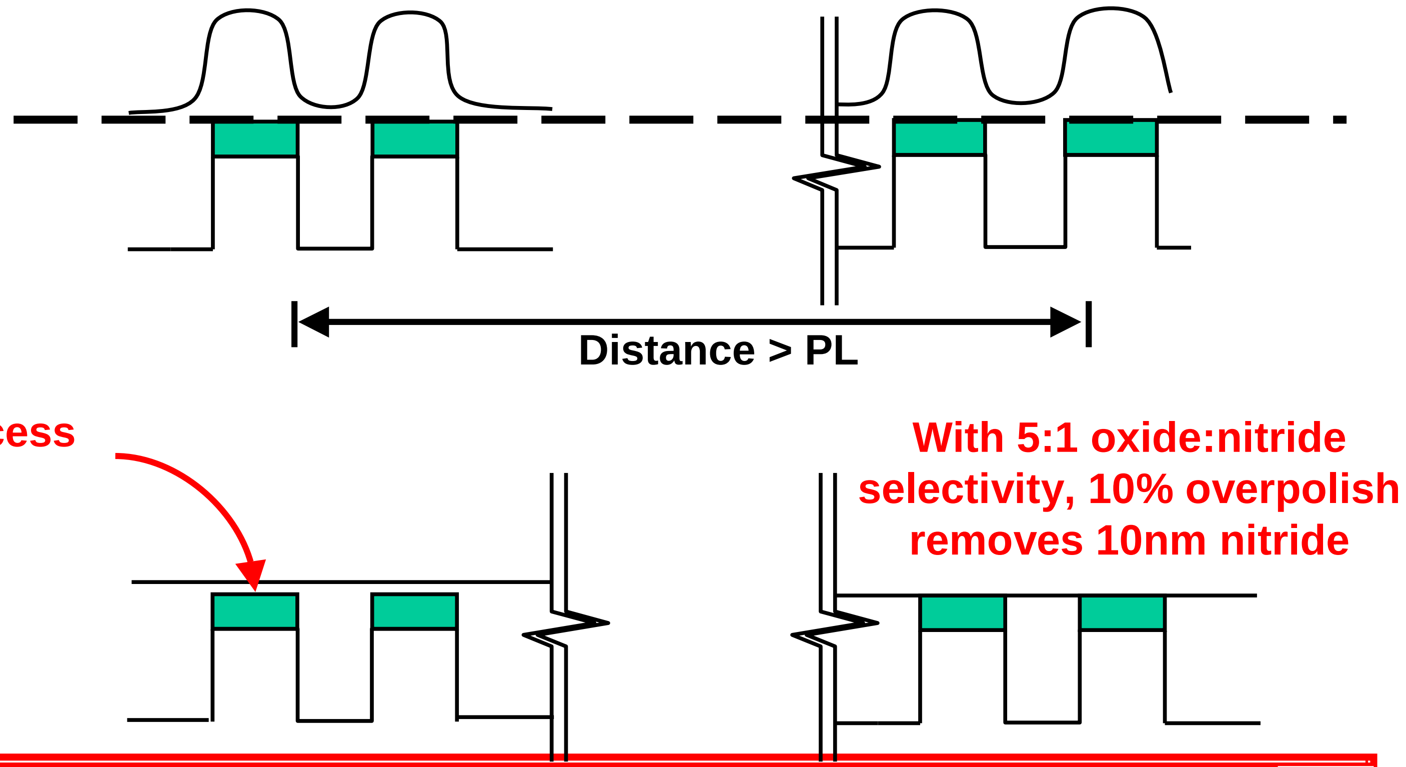
Problem #2: Excessive Nitride Thinning

- To clear oxide, one must over-polish substantially
- Because the CMP pad/process does not bend into recessed region, one must over-polish into the nearby nitride in order to clear oxide



Compare: Wafer Level Rate Nonuniformity

- Consider 500nm oxide step; 5% rate nonuniformity over 200mm wafer
- Variation occurs over distance > PL, so pad can remove oxide without excessive nitride thinning



20mm chip; right side polishes 0.5% faster

Pre-CMP

Distance > PL

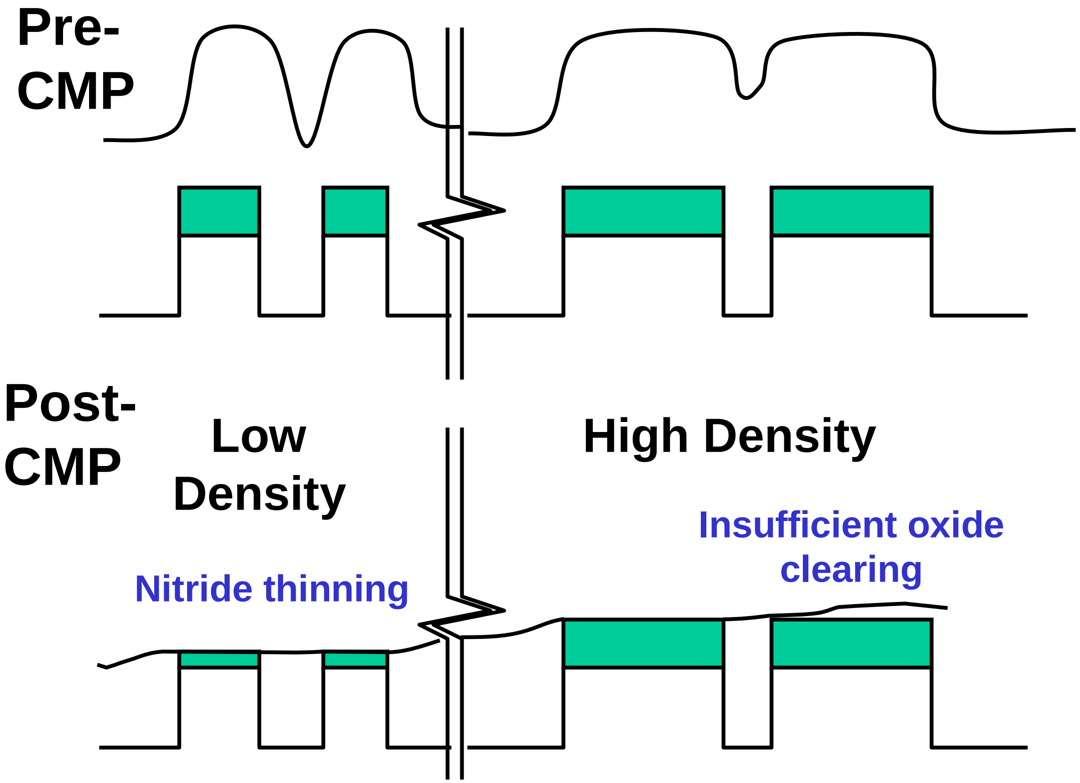
Leaves 2.5nm excess oxide to clear

With 5:1 oxide:nitride selectivity, 10% overpolish removes 10nm nitride

Post-CMP

Compare: Pattern Density Effect

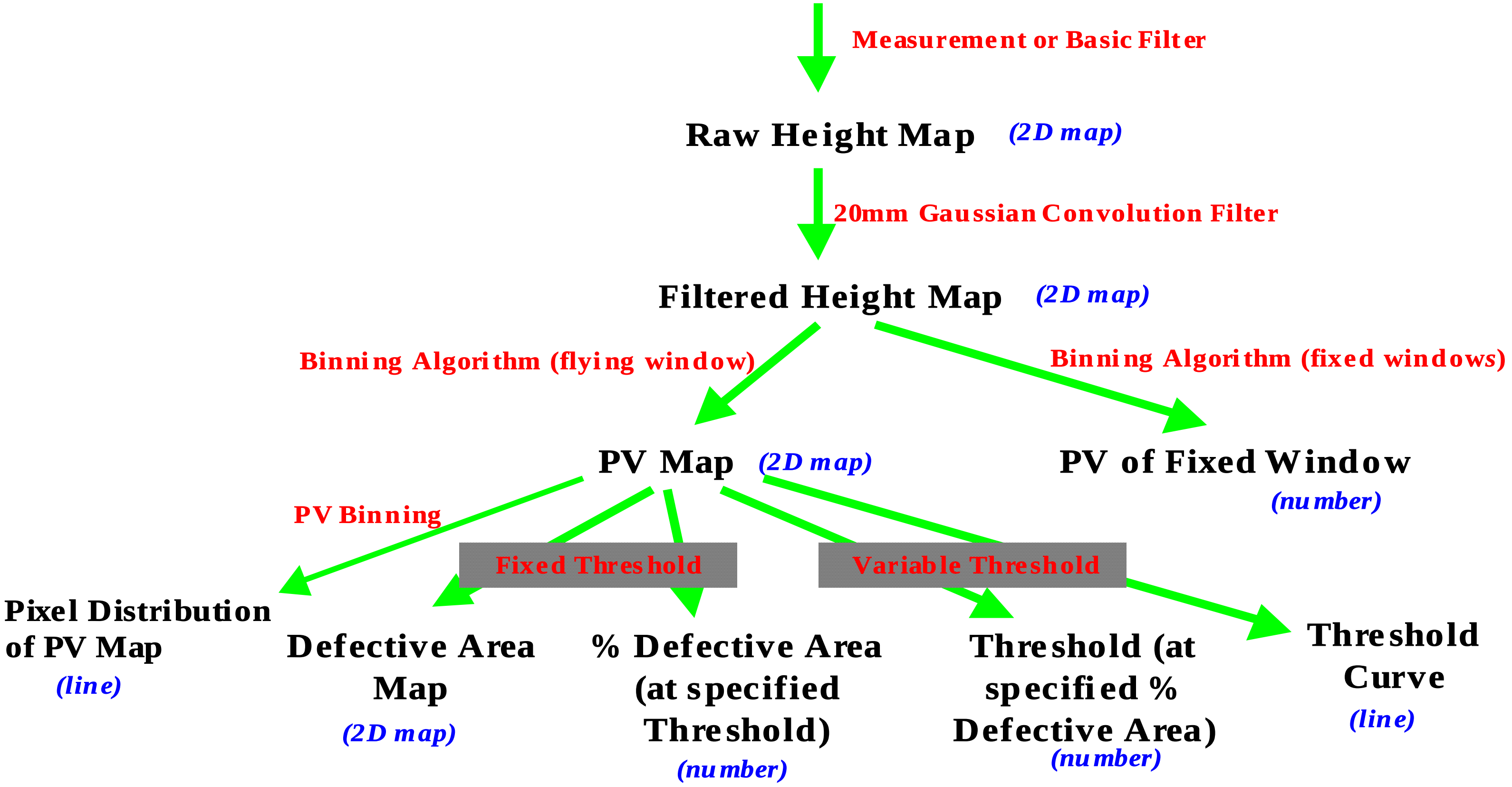
- Regions with different pattern densities will polish at different rates, leading to uneven clearing of overburden oxide across the chip
- Serious concern attacked by:
  - – dummy fill
  - – oxide:nitride selectivity
  - – moving to stiffer pads to better average density ⇒ worsens nanotopography effect!



Conclusions

- Nanotopography can be a serious concern for STI, depending on the specifics of the nanotopography and the CMP process
- CMP process planarization length (PL) is key parameter affecting how thin films over nanotopography evolve during polishing
- Approaches to modeling this effect: density and/or contact wear
- Nanotopography/CMP experiments
  - Wafer splits: range of nanotopography length scales
  - Process splits: range of planarization lengths
  - Preliminary results: data supports hypothesis – PL vs. NL
- Future work
  - Full data analysis and modeling
  - Implications for nanotopography metrics
  - Modeling and experiments to study nanotopography impact on STI structures

Nanotopography Metrics



Measurement or Basic Filter

Raw Height Map *(2D map)*

20mm Gaussian Convolution Filter

Filtered Height Map *(2D map)*

Binning Algorithm (flying window)

Binning Algorithm (fixed windows)

PV Map *(2D map)*

PV of Fixed Window *(number)*

PV Binning

Fixed Threshold

Variable Threshold

Pixel Distribution of PV Map *(line)*

Defective Area Map *(2D map)*

% Defective Area (at specified Threshold) *(number)*

Threshold (at specified % Defective Area) *(number)*

Threshold Curve *(line)*

AT Center Munich, ADE International GmbH

Dr. Lars Wende - July 6, 2000