DETERMINATION OF THE PLANARIZATION DISTANCE FOR COPPER CMP PROCESS

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ABSTRACT

A previously published planarization monitor which had been applied to oxide CMP is extended to the copper system to investigate pattern dependencies during copper overburden planarization. Conventional profilometry and a noncontact, acousto-optic measurement tool, the Insite 300, are utilized to quantify the planarization performance in terms of the defined step-height-reduction-ratio (SHRR). Illustrative results as a function of slurry, pad type and process conditions are presented. For a typical stiff-pad copper CMP process, we determined the planarization distance to be approximately 2mm, comparable to that reported in oxide CMP.

INTRODUCTION

Copper has emerged as the leading contender for back-end-of-line metallization for advanced integrated circuits. Lack of a viable copper etch process and depth-of-focus limitations of advanced lithography leads to the chemical-mechanical polishing (CMP) of Damascene structures as the preferred method by which copper-based metallization is formed. CMP is the only known feasible method by which copper metallization can be patterned to the requisite, feature size and global planarity.

The primary polish metrics characterizing the topography generated during the CMP of metal Damascene structures are the dishing of wide metal lines, erosion of dense metal arrays and thinning of the dielectric field region. Erosion is a primary issue at the lower levels of metallization where high metal pattern-density, narrow linewidth structures are formed. Dishing is more prominent at the upper metal layers where single structures of greater area (bus lines and bond pad structures) are present. The associated film thickness reductions will influence the circuit performance through line resistance, interlevel and intralevel capacitance variation [1]. Thus, care must be taken to ameliorate such issues, which stem from both plating and polish process limitations.

For the aggressive topographies of next generation integrated circuits, electroplating is a viable fill technique. However, both 'feature-scale recess' of wide structures and 'array-scale recess' can be significant. Figure 1 displays the as-plated array recess as a function of metal pitch for a 50 % metal density array showing over 2000 Å recess in some cases. Such as-plated single feature and array length-scale topographies will directly influence the CMP performance. A strong drive exists to develop plating processes with small as-plated topography on both the individual feature and array dimensions while maintaining desired across wafer uniformity and fill capabilities. The central concern of this paper is to examine the ability of CMP to planarize as-plated copper topography.

Previous work has examined pattern-dependent planarization issues in oxide CMP processes. The polish rate at a specific site on a patterned wafer has been modeled as an appropriately weighted function of the pattern density over a characteristic region defined by the 'planarization length or distance' [2,3]. Such models assumed perfect planarization efficiency and led to linear step height reduction with time relationships. Models which incorporate compressible pads and partial loading of the down regions led to exponential step height reduction with time relationships after the initial linear component [4]. These models, however, neglect changes in effective pressure due to global non-planarity created by topography. An example of this effect occurs during the polishing of next-level metal which incurs preexisting topography as a result of array erosion at the previous level as shown in Figure 2. The resulting array serpentine lines after polish are thicker as a result of initial recess and shielding by the neighboring field region which lowers the effective pressure on the array.

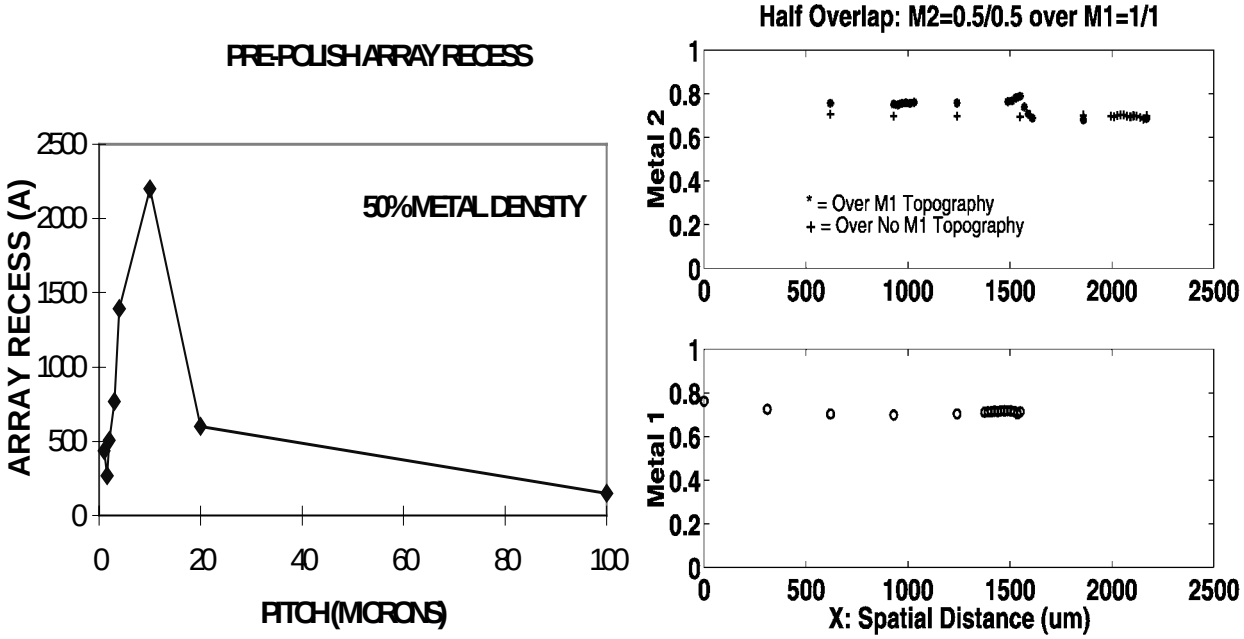


Figure 1 'Array-Scale Recess' resulting from a copper electroplate process over a 50% metal density, 2500μm x 2500μm array as a function of pitch.

Figure 2 Comparison of array metal thickness for an initially recessed array at M2 due to M1 induced topography versus the same array at M2 over M1 field. Field dielectric shielding at M2 reduces M2 array erosion for the initially recessed structures.

In copper CMP processes, two measures are important in characterizing the initial copper removal. The planarization distance indicates the length scale over which raised topography interacts. The planarization efficiency indicates the amount of topography that must be removed to eliminate an existing step height. After the initial copper removal, the CMP process processed with barrier film removal, and during clearing across the wafer also results in erosion and dishing in the multicomponent material system (copper-barrier-dielectric). The resulting within-die total-indicated-range (TIR) of a patterned wafer after CMP is a function of both copper overburden and subsequent dishing and erosion: non-ideal planarization of the as-plated copper topography further contributes to dishing and erosion difficulties.

The initial part of the polish process can thus be viewed as acting to remove preexisting topography while the latter clearing stage aims to prevent the generation of topography. Polish processes having large planarization distances are more effective at both the single feature length

scales associated with as-plated line-recess and conventional dishing during the clearing stage as well as the more difficult to planarize array-recess from the plate process and conventional array erosion from barrier clearing during CMP. The planarization efficiency is in general a monotonic function of length scale, worsening with increasing dimension due to pad bending. As the planarization distance of a CMP process increases, the local polish rate becomes increasingly dependent upon the neighboring real estate through the effective pattern density. When the planarization distance becomes much larger than the die size, the effective pattern density becomes a constant and the die is polished the same everywhere (neglecting higher order effects). Harder, stiffer pad processes typically have planarization capability well into the mm-length scale regime, with soft, flexible pads only able to planarize into the 100-micron regime. Hence, in the presence of as-plated array-recess, a hard pad process is desirable.

The planarization quotient has been used to gauge the global planarization capability of an oxide CMP process using a previously published planarization monitor [5]. The derived S-shaped, planarization quotient vs. feature size curve leads to determination of the planarization distance of a given oxide CMP process and allows comparison of the oxide CMP performance between polish platform, process conditions and consumables sets. In this paper, we report the evolution and quantification of a related parameter, the step-height-reduction-ratio, and subsequently extract the planarization distance for copper CMP for the first time. Conventional profilometry and the InSite300™ photo-acoustic measurement tool were employed to quantify copper film thickness and topography. The Insite 300™ operates upon the transient gradient technique and allows for noncontact, nondestructive metal film thickness measurement [6]. The utility of this metal thickness tool bypasses a number of issues which arise with conventional profilometry. The ability to accurately delineate metal feature edge positions and circumvent stress-induced curvature present in long profilometry scans is of principle importance.

EXPERIMENT

The planarization test vehicle is comprised of a set of 18 trenches etched in 200mm dia. Si wafers to the depth of 0.8 μm with the trench set replicated twice per wafer. All trenches were 8.0 mm long, with the width varying from 0.1 mm to 8.0 mm. The 0.1mm structures can be viewed as representing the individual feature performance (dishing of a 100μm wide square) and the higher length scales can be viewed as applying to erosion or array recess effects. The intent was to provide sufficient separation between the trenches in order to isolate each particular structure. However, for the widest structures, the field length was less than 6 mm and the structures begin to interact for processes with a large planarization distance. Additionally, an error in lithography affected some of the larger structures and is discussed later. After silicon etching, a blanket 20 kÅ TEOS layer was deposited followed by 250 Å Ta barrier/1000 Å Cu seed/1.5μm electroplate copper metal film stack. Subsequently, CMP of only copper film (without breakthrough to the underlying barrier or oxide) was performed under a variety on conditions. Films were characterized by either the profilometer or the photo-acoustic tool after each CMP. The resulting step-height after CMP at the middle of the trench relative to the field value at a trench-width distance away was then derived.

RESULTS

Profilometry was performed on a wafer which was polished in 40 second time increments under baseline conditions using an experimental grade copper slurry at 4 psi on a perforated IC1000/Suba IV pad on an IPEC 372MU. Figure 3 displays the extracted step-height-reduction as a function of trench width. Several important conclusions are immediately evident.

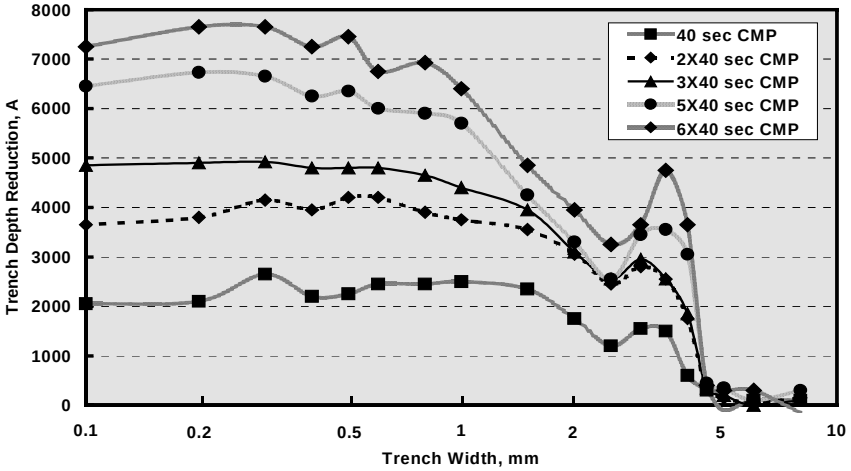


Figure 3 Trench Depth Reduction vs. Trench Width for equal time polish increments

First, no planarization is achieved for feature sizes above 4.5 mm. For feature sizes 1.0 mm to 4.5 mm, only partial planarization is possible, and with the exception of the 3, 3.5 and 4 mm structures, its effectiveness increases monotonically with feature size reduction. And finally, for feature sizes 1.0 mm and below, nearly constant planarization efficiency was achieved, as the trench depth was reduced from 0.8 μm to zero. We believe that the irregularity in our experimental data for 3-4 mm feature sizes was caused by an error in the exposure. This caused each of these structures on wafers from this particular lot to be actually composed of two smaller trenches with slight separation, as evidenced from visual inspection of the pre-polished wafers.

We define the planarization efficiency (PE) in terms of the step-height-reduction–ratio (SHRR), which is the SHR normalized by the amount removed (the maximum SHR value). The planarization distance (PD) is then defined as that length value for which the PE equals a fixed value, e.g. 0.3. This also appears to be the length value at which the inflection point resides. For each polish increment, the inflection point remains on the order of mm as shown in Figure 3, though there does appear to be a slight shifting to lower value. The PD can be viewed as the capability or distance over which the system can planarize, while the PE is a measure as to the speed at which planarization is performed. Based on the data presented in Figure 3, we determined the planarization distance for this copper CMP process to be approximately 2 mm, which is comparable to reported planarization distances of oxide CMP processes using similar process configuration [7].

Numerous difficulties arose in performing profilometry on the as-polished wafers in some cases. Substrate curvature and feature rounding leading to difficulties in referencing the step edge were two key issues which led to investigation of an alternative metrology approach. Figure 4 displays the associated thickness plots across the full range of structures on the test vehicle using the Insite 300 direct metal thickness measurement tool.

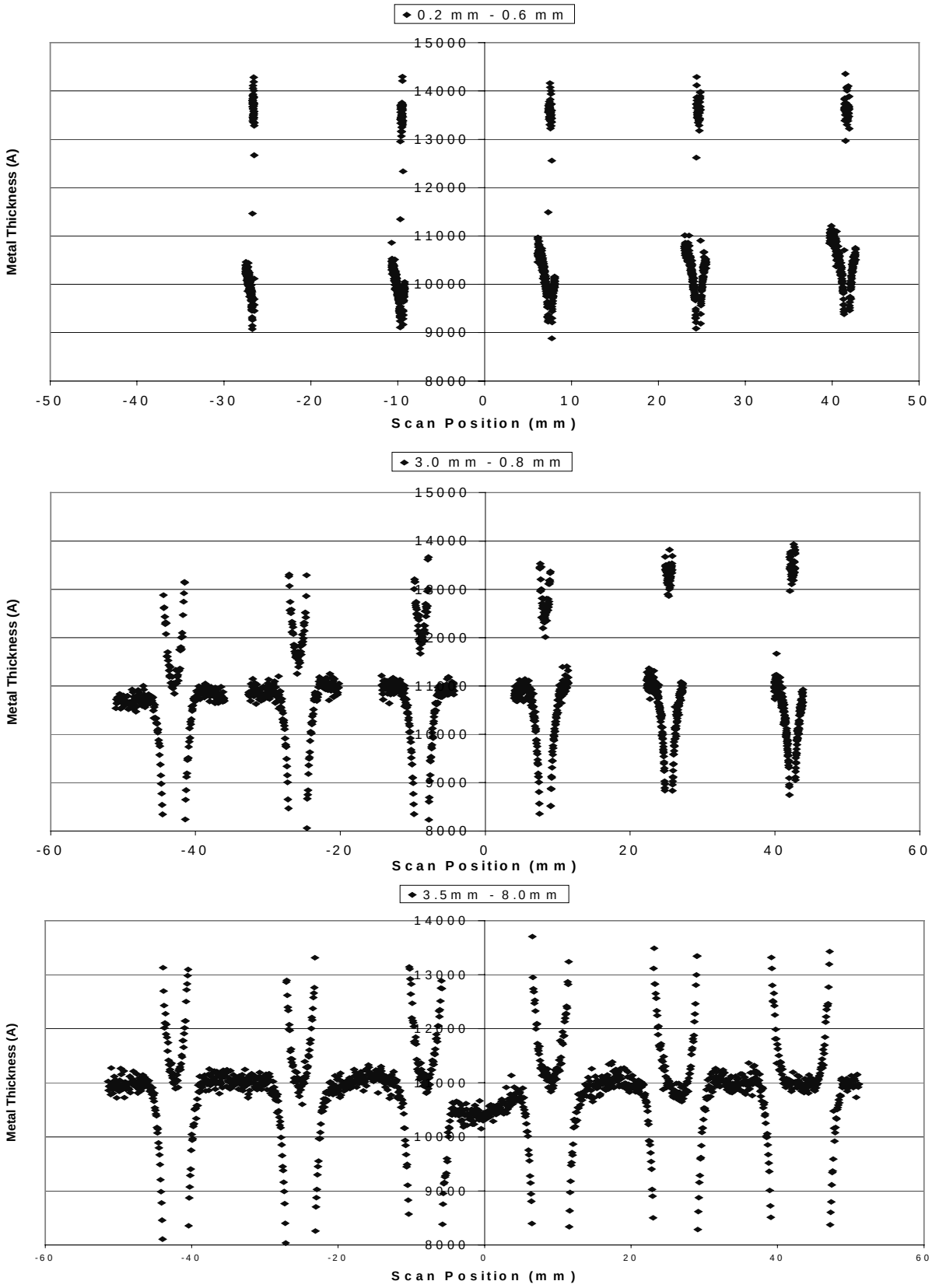
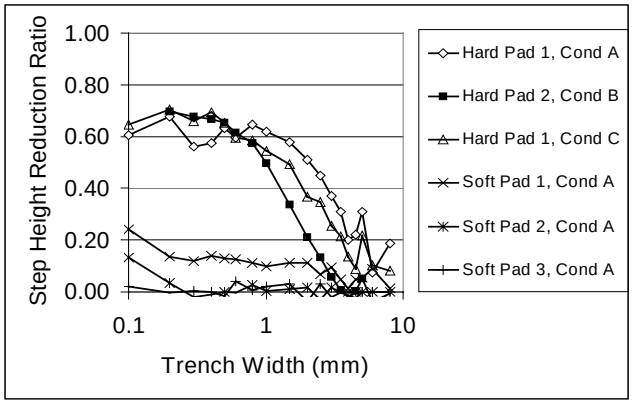


Figure 4. Insite 300 Metal Thickness Scans across the features of the Test Vehicles

In Figure 4, the trench edge corresponding to the position of copper thickness discontinuity is clearly visible. As one moves from the field region toward the edge of a trench the thickness decreases; inside the trench the copper is thicker (protected) if planarization is successful. We see from Figure 4 that substantial planarization takes place for small trenches while for 3.0 mm and larger trenches the copper thickness at the center of the trench is comparable to the copper thickness in the field. Based upon these measurements the SHRR is derived.

Figure 5 contrasts the SHRR results from a set of runs on different pads using various process conditions. Hard pads are seen to offer significantly higher SHRR than soft pads over the entire trench space and the associated PD is significantly higher. The process conditions influence the SHRR as well, but to lesser degree than the pad. Figure 6 displays the associated SHRR data for monitors polished using two different slurries. For Slurry 2, the SHRR seems to be limited by slurry performance in the low trench width regime, while the hard pad limitation shows its SHRR limitation at larger trench widths.



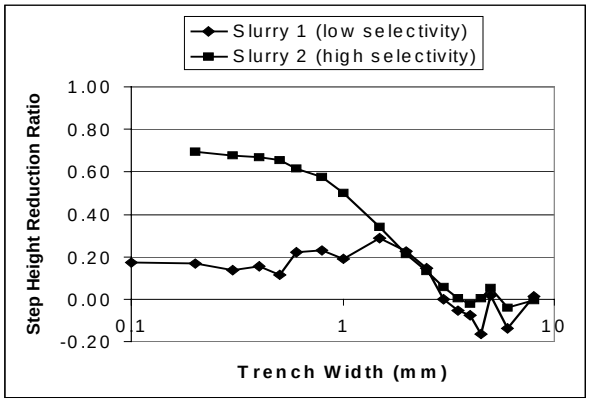


Figure 5 Metal Thickness Difference vs. Trench width for different pad-process combinations

Figure 6 Metal Thickness Difference vs. Trench Width for two different slurries

CONCLUSION

Using a previously published planarization monitor, the planarization efficiency and planarization distance were computed for a copper CMP process. The influence of polish pad, slurry and process conditions was demonstrated. Results indicate that harder, stiffer pads can extend planarization performance to wider structures given a suitable choice of slurry. Process conditions play a relatively minor role. The planarization of copper during the as-plated copper overburden removal was found to exhibit similar behavior to the planarization of oxide topography in oxide CMP, with a planarization distance of approximately 2mm for a typical stiff-pad copper CMP process.

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