Future Fab International, December 1996.

Statistical Metrology: Tools for Understanding Variation

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ABSTRACT

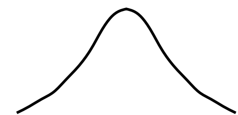
As parametric variation increases in importance with shrinking dimensions and increasing integration, the need to understand and manage such variation is becoming critical. Statistical metrology is a collection of tools and techniques for the systematic characterization and study of variation in semiconductor manufacturing. In addition to methods for collecting large volumes of data, important analytic approaches are being developed (1) to decompose parameter distributions into wafer-level, die-level, and wafer-die interaction contributions; and (2) to model the spatial effect of layout, process, or other factors on observed variation. Statistical metrology has been used to study interlevel dielectric thickness and polysilicon critical dimension variation, and new applications to yield improvement, design rule generation, and variation impact analysis will make statistical metrology an important part of future manufacturing and design practice.

1. INTRODUCTION - PARAMETRIC VARIATION

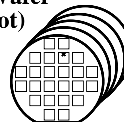
Parametric variation is an increasing concern in integrated circuit fabrication. Stringent control of both device and interconnect structures, such as polysilicon critical dimension (channel length) or interlevel dielectric thicknesses is critical not only for adequate yield, but also to achieve increasingly aggressive performance and reliability requirements. Understanding and assessing such variation, however, is difficult: variation may depend on process, equipment, and specifics of the layout patterns all confounded together. Here we discuss an emerging "statistical metrology" approach which provides tools and techniques for measuring, isolating, and modeling *variation* in semiconductor manufacturing [1, 2, 3]. We will first discuss the nature and scope of parameter variation under study, and then describe experimental design and analytic tools for understanding this variation. Finally, we examine current and future applications of statistical metrology to solve manufacturing and design problems.

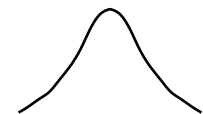
Variation in some physical or electrical parameter may manifest itself in several ways. One key characteristic of variation is its scope in time and in space, as shown in Figure 1, where we see that the variation appears at a number of different scales. The separation of variation by unique signatures at different scales is a key feature enabling one to analyze such variation. Process control has often been concerned with variation occurring from lot-to-lot or wafer-to-wafer. That is, some measure of a parameter for the lot may vary from one lot to the next as the equipment, incoming wafer batch, or consumable material drifts or undergoes disturbances. In addition to temporal variation, different spatial variation occurs at different scales. In batch processes, for example, the spatial variation from one wafer to the next (e.g. along a polysilicon deposition tube) may be a concern. In equipment design and process optimization, spatial uniformity across the wafer is a typical goal and specification. For example, in most deposition or etch processes, uniformity on the order of 5% across the wafer can be achieved; if one examines the value for some structural parameter taken at the same point on every die on the wafer, a fairly tight distribution results. At a smaller scale, on the other hand, additional variation issues may arise. In particular, the variation within individual die on the wafer is emerging as a major concern, in large part because of potential yield and circuit performance degradation. An important observation is that knowing something about one scale of variation says little about the variation at the other scales. This is because different physical causes are at work at each scale; e.g. wafer level uniformity in plasma etch is driven by macroscopic tool design issues, while die-level pattern-dependencies (which may in fact be larger than wafer variation) arise through details of the etch process conditions.

Lot–to–Lot

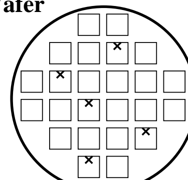


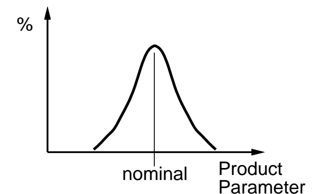
Wafer–to–Wafer (or within Lot)





Within Wafer





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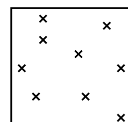

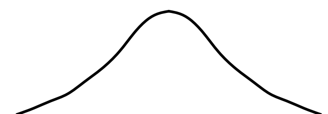

Figure 1. Spatial and temporal variation scales.

The second key characteristic of variation is systematic versus random constituents in the parameter distribution. An important goal is to isolate those systematic, repeatable, or deterministic contributions to the variation from a set of deeply confounded measurements. A set of dielectric thickness measurements from many locations on one wafer following planarization by chemical mechanical polishing is collected; without detailed understanding of the individual contributions, the resulting distribution, shown in Figure 2, might be considered to be "random" and large. Better understanding of the specific contributions to the distribution enables one to focus variation reduction efforts more appropriately, or to design the device or circuit to compensate for the expected variation.

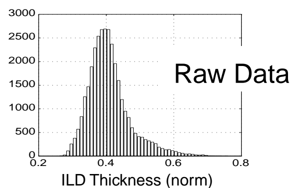

Figure 2. Histogram of normalized ILD thickness measurements taken on a wafer following oxide CMP.

2. TEST STRUCTURE AND EXPERIMENTAL DESIGN

Analysis and deconvolution of spatial variation requires carefully designed test structures and experiments. For example, electrical test structure to study the dependence of ILD thickness on line width or other layout factors should examine different combinations of these layout factors [4]. Test chip and short flow experimental loops are an integral part of statistical metrology. For example, screening experiments which explore a large number of factors [4], or environmental/modeling experiments which mimic realistic circuits [5], can be designed as illustrated in Figure 3. Once fabricated, large volumes of electrical or optical data can be collected to enable variation analysisVARIATION ANALYSIS

2.1 Variation Decomposition

The first stage in analyzing parameter variation is to break that variation down into smaller components which correspond to typical variation sources. In particular, spatial variation will usually consist of wafer-level (or across-wafer) variation and die-level (or within-die) variation, as well as other elements. As pictured in Figure 4, statistical and signal processing methods can be employed to utilize the different spatial scales of these variations to achieve decomposition [6]. The second stage can then proceed, in which the functional dependencies of the variation can be explored and modeled. The variation decomposition approach of Figure 4 can be expressed in the framework of an additive model [7] in which the total variation is represented as the sum of individual variation terms:

$$\begin{aligned} f_{RAW} &= f_{WLV}(x, y) + f_{DLV}(x, y) + f_{WLV \otimes DLV}(x, y) + \varepsilon \\ & \quad where \qquad \varepsilon \sim N(0, \sigma^2) \end{aligned} \quad . \quad (1)$$

In Equation 1, x and y are spatial coordinates on the wafer while f_{WLV} is the wafer-level variation, f_{DLV} is the die-level variation, $f_{WLV \otimes DLV}$ represents the wafer-die interaction terms, and ε corresponds to the residual terms. Variation decomposition is able to (1) identify systematic spatial components in the variation, and (2) quantify these variation components.

Consider again the ILD thickness measurements from Figure 2. Knowing the spatial location of those measurements enables the estimation of wafer-level variation by a variety of methods include moving average filters, spline-based approaches, and regression to assumed parametric forms [6]. These approaches take advantage of assumptions on the shape of such variation: gradual trends are typical, or known functional forms are used (e.g. radial dependencies, sloped planes, or combinations of these). The wafer level ILD variation extracted using a moving average estimator is shown in Figure 5. Also shown in Figure 5 is the extracted wafer level variation for the same test mask planarized on a different CMP tool type; the resulting wafer level variation is very different, consisting of a "slanted plane" nonuniformity.

When die-level spatial dependencies are examined, the key assumption is that the intended chip pattern imposes repetition among the many die on any one wafer. The decomposition methods exploit this repetition. Spatial repetition imposed by the stepping of the die across the wafer suggests the use of frequency-based analysis methods. A 2D spatial Fourier transform approach [3], for example, results in isolation of those components corresponding to the fundamental die frequency and its harmonics. In the case of our ILD variation example, the resulting "die signature" for the particular mask used in shown in Figure 5. This extracted die pattern is exactly the same for all die on the wafer, but may vary from one wafer to the next under the influence of other conditions. Also shown in Figure 5 is the die-level variation pattern resulting from polishing an a different tool type; while the two wafer-level nonuniformities are very different, the die-pattern signatures are nearly identical. .

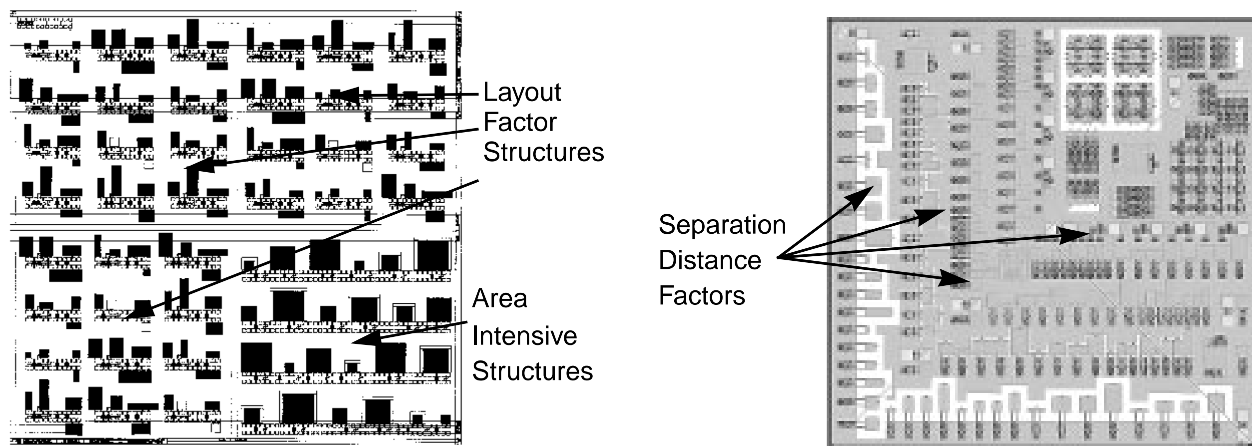

Figure 3. Example test chip experimental designs. A screening experiment (left) explores the influence of local layout factors on the ILD thickness of individual structures. An environmental experiment (right) more closely mimics an ASIC layout, and also explores the effect of separation distance between structures and nearby dummy fill.

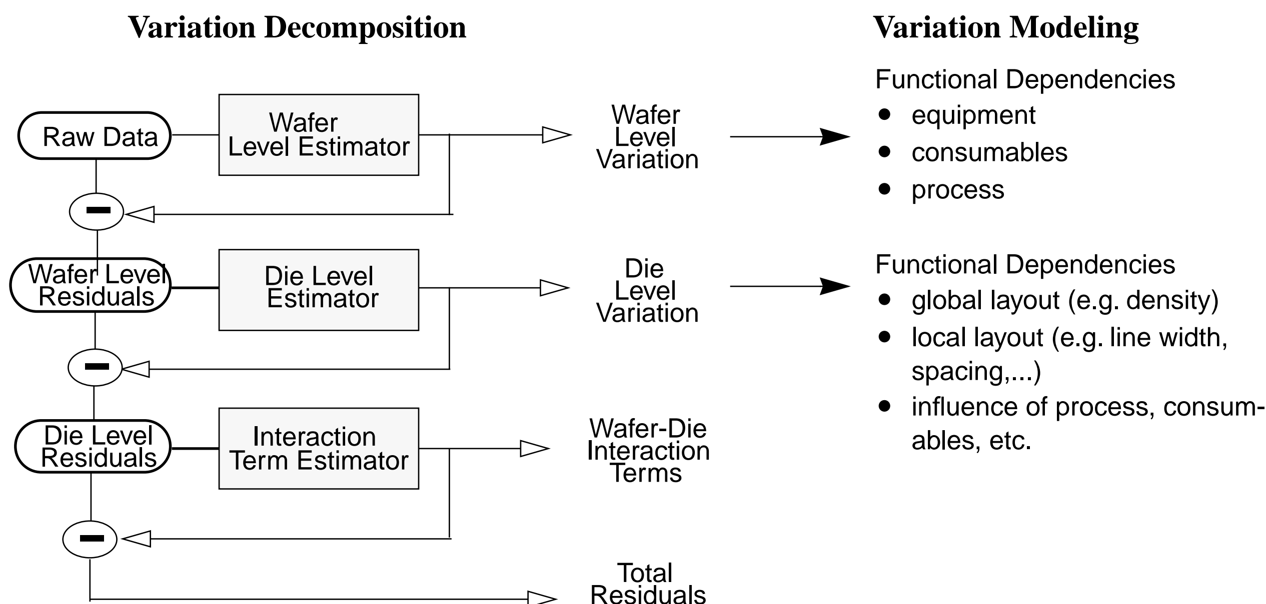

Figure 4. Variation Decomposition and Modeling Flow Diagram

An important interaction may occur between the “pure” die level variation pattern and wafer-level dependencies. For example, the die-level pattern may be attenuated or accentuated depending on the location of the die on the wafer. At the wafer scale, the center of the wafer is often better controlled and more uniform, while the edges of the wafer experience significant “bull’s eye” or other nonuniformities. As a result, the die-level pattern dependencies may be significantly worse near the edge of the wafer. If one is concerned about the total range of variation, then, a multiplicative or other interactive factor between the die-pattern and wafer location may be a very large concern. More work is needed to understand the relationships between the interaction and the constituent die and wafer components. Spatial modeling approaches include methods which examine the residuals in Figure 4 for remaining quasi-periodic energy [6], or that use modified ANOVA models that mix factor and spatial location effects [8]. In the case of poly critical dimension, a multiplicative model has been proposed by Yu et al. [9] to account for wafer-die interaction.

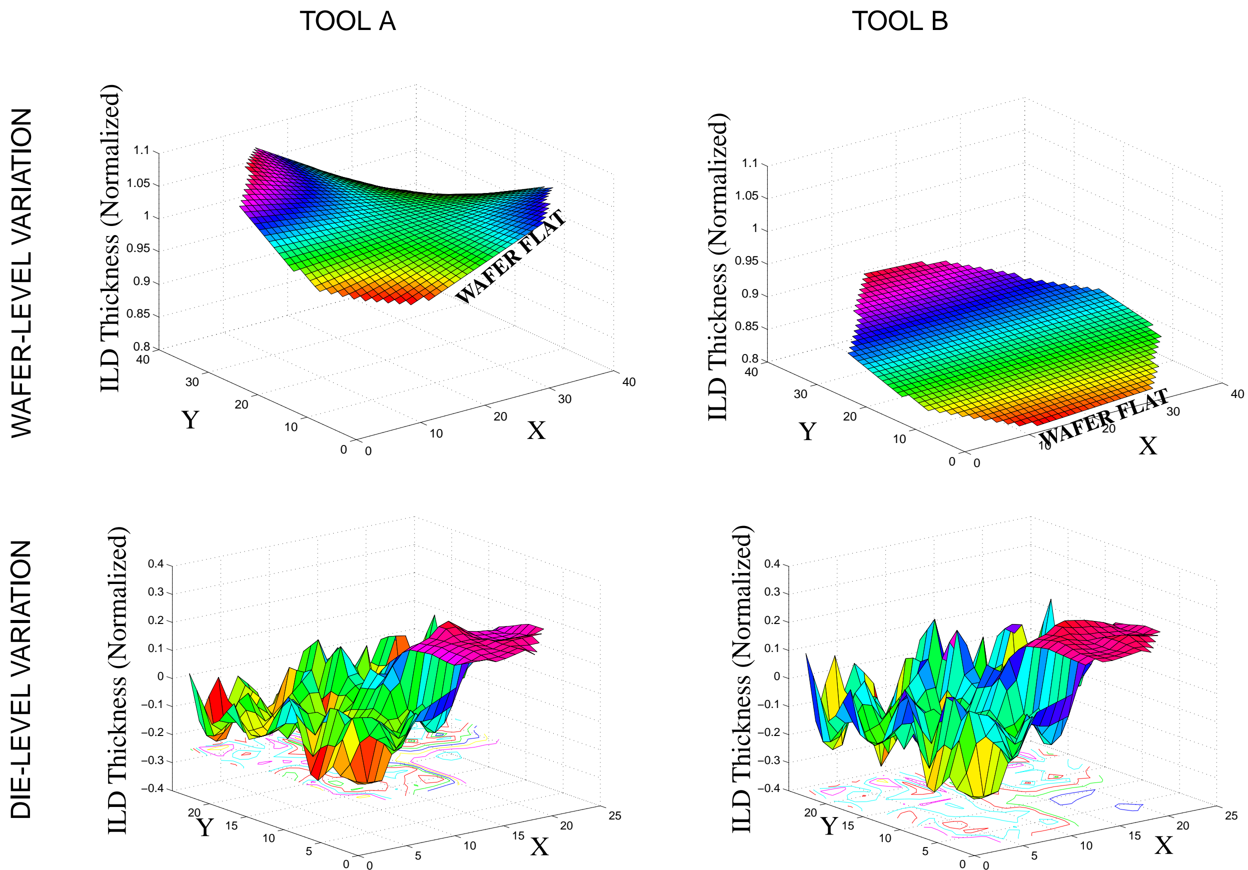

Figure 5. Comparison of wafer and die-level variation for two different CMP tools.

The decomposition approaches as outlined above are summarized in Figure 6 which shows the wafer, die, and wafer-die variation distribution in (normalized) ILD thicknesses resulting from deconvolution and decomposition. It is important to note that the wafer, die, and wafer-die distributions are not random; the complicated shape of these distributions are a function of the variation itself as well as the test structure and experimental design factors used to study them. On the other hand, the residual component contains both truly random variation or other variation factors not comprehended in the analysis.

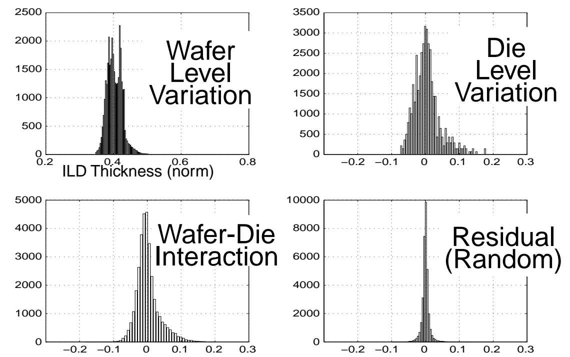

Figure 6. Components of ILD thickness variation after variation decomposition corresponding to the raw data in Figure 2. The wafer, die, and wafer-die histograms correspond to systematic components in the raw data, while the remaining narrow residual component is random.

2.2 Variation Modeling

The methods described above enable the decomposition of variation into different components. While such decomposition alone is very useful in directing reduction efforts, comparing equipment, and gaining insight, it is also desirable to build explicit models that capture the functional dependency between the parameter of interest and the contributing factors. Methods for such modeling are just beginning to emerge in statistical metrology. One approach is to examine the extracted die-level variation for factor dependencies, where the factors are typically related to features of the layout or chip pattern (e.g. line widths, line spacing, orientation of features, proximity to nearby structures, etc.). A simple analysis of variance (ANOVA) approach can be used to compare the influence of individual factors, explore interactions between those factors, and construct models [4]. Manipulation of the underlying factors may be appropriate to construct good models. For example, the line width and line spacing factors in ILD thickness variation studies may be efficiently modeled in terms of local or global layout density parameters, resulting in a compact model as pictured in Figure 7. Empirical models such as these can feed design rule generation (e.g. specify required layout density to bound within die topography ranges), or can be integrated into quasi-empirical simulation tools.

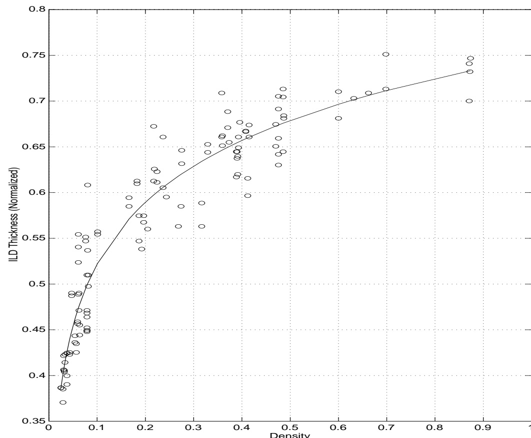

Figure 7. Model of ILD thickness as a function of layout density, constructed by analysis of data from the (right) test die in Figure 3.

The development of methods for simultaneous modeling of pattern and spatial dependencies is an active area of research. A modified ANOVA approach which captures both the systematic (repeatable or shared) die-level variation and the die-wafer interaction terms has recently been proposed [8]. In this approach, ANOVA models are constructed for each die of interest, and then the ANOVA coefficients are compared and analyzed for their spatial dependencies. For example, the analysis of polysilicon critical dimension (poly CD) and its relationship to Id_{SAT} variation is crucial to understanding chip or circuit performance impact. For each measured die, an ANOVA model:

$$Id_{SAT} = \mu + \begin{Bmatrix} \alpha_F \\ \alpha_I \\ \alpha_S \end{Bmatrix} + \begin{Bmatrix} \beta_H \\ \beta_V \end{Bmatrix} + \begin{Bmatrix} \gamma_{WIDE} \\ \gamma_{NARROW} \end{Bmatrix} \qquad (2)$$

is developed where μ, α_F, α_I, α_S, β_H, β_V, γ_{WIDE}, and γ_{NARROW} are constants which are fitted to the data. In this type of model, the expected Id_{sat} value for a particular transistor with a given set of layout factors is determined by selecting the appropriate constant term from each brace and adding each term together. For example, if a transistor is isolated, horizontally oriented, and wide, then the expected Id_{sat} value is $\mu + \alpha_I + \beta_H + \gamma_{WIDE}$. A typical ANOVA model (normalized) for a die near the center of the wafer is:

$$Id_{SAT} = 0.409 + \begin{Bmatrix} 9.375 \\ 10.630 \\ 1.254 \end{Bmatrix} + \begin{Bmatrix} -3.162 \\ 3.162 \end{Bmatrix} + \begin{Bmatrix} -1.641 \\ 1.641 \end{Bmatrix} \qquad (3)$$

and the ANOVA statistics for this particular die are shown in Table I. The ANOVA table reveals that spacing (fingered vs. isolated vs. stacked) and geometric orientation (horizontal vs. vertical) are the most significant layout factors while channel width is not significant as judged by the Pr(F) column (under a few assumptions of normality, there values indicate the probability that the observed differences between groups could have arisen by chance alone). The model coefficients, μ, α_F, α_I, α_S, β_H, and β_V, can also be examined as a function of die spatial location on the wafer. By looking at the spatial dependence of each factor type (e.g. geometric orientation versus spacing in this particular case), possible different physical and spatial dependencies can be highlighted. For example, in this case it was found that isolated poly CD lines have a positive dependence on radial wafer position while the stacked and fingered devices have a negative dependence on radial position. More methods are needed that mix factor modeling with spatial distribution or

Table I. ANOVA Table for Id_{SAT} model related to poly CD layout factors for an example die, corresponding (3)

Factor	DF	Sum of Sq.	Mean Sq.	F-value	Pr(F)
spacing	2	6964	3482	81.41	0.0000
geom. orient.	1	745.8	745.8	17.44	0.0003
width	1	56.8	56.8	1.32	0.2614
Residuals	22	940.96	42.77	-	-

Table II. Statistical metrology applications.

Application	Examples
Equipment Characterization/Evaluation	Steppers/lithography [9]
	Chemical-mechanical polishing [4], [5], [10]
Equipment/Consumable Optimization	
Process Synthesis & Optimization	Causal decomposition: litho, etch contributions to CD variation [12]
	Spatial modeling of defect patterns [14]
Process/Equipment Control	Generation of control requirements [18]
Layout Optimization	Dummy-fill patterning practices for CMP [13]
Circuit Impact/Optimization	Ring oscillator frequency as function of within chip poly CD variation [15]
	Within chip transistor variation correlations and clock speed impact [16]
	Process variability and device mismatch [17]

parameter dependencies on other factors, including time, process parameters, or other exogenous variables.

3. STATISTICAL METROLOGY APPLICATIONS

Statistical metrology is providing new tools and methods to guide the design of valid experimental designs and collection of data, to support the decomposition and modeling of the variation (spatial variation in particular), and to study the impact of that variation on manufacturability, performance, and reliability. Table II summarizes several areas where statistical metrology can be applied. One early application of statistical metrology is "fingerprinting" or characterization and comparison of different equipment sets. For example, the impact of different steppers on die-level line widths has been examined [9], and comparisons between typical wafer and die-level patterns in oxide polish using different CMP tools have been reported [10]. Such studies are immediately useful in equipment selection decisions, but can also be used to guide equipment or consumable optimization. Indeed, in CMP there is a strong demand for a "standard" means of characterizing spatial and pattern dependent performance of difference slurry or pad designs [11]; statistical metrology can supply experimental design and analysis methods for such standards. In addition to characterization and optimization of the equipment, variation models are needed to guide process optimization and process synthesis. Short-flow methodologies are needed that can accurately characterize the performance of process modules, including their important variations and interactions, so that full flow processes can be more rapidly and easily assembled. An important element of this is the causal decomposition of variation - identifying the process steps or modules that contribute to overall variation. For example, the contributions of etch and lithography in line width variation have been studied by Yu et al. [12]. Once process design has been accomplished, there is a critical need for process and equipment control strategies that can monitor and minimize such variation. For example, any modification to process parameters in a production process, be they as simple as polish time or as sophisticated as full multivariate process control, will be undertaken only when the die-level variation implications of that change are well understood.

In addition to application in the manufacturing arena, statistical metrology will play an important role in product design as well. Statistical metrology can contribute to variation reduction through improved circuit design practice. In the case of CMP, for example, the experimental methods and models of ILD thickness variation dependencies on layout patterns are already contributing strongly to the development of metal fill patterning practices [13]. An important future opportunity is the use of variation models to design circuits which are robust to or compensate for known systematic variation sources (e.g. skew differences due to systematic ILD thickness variation).

ACKNOWLEDGMENTS

We would like to acknowledge the many contributions of students, staff, and industrial collaborators, including colleagues at MIT, HP, Sandia National Laboratories, LSI Logic, Digital Semiconductor, PDF Solutions, and Texas Instruments. This work has been supported in part by DARPA under contract #DABT-63-95-C-0088 and AASERT grant #DAAHA04-95-I-0459.

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