Copper CMP and Process Control

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ABSTRACT

A production worthy, copper CMP technology has been successfully developed on a multi-platen CMP system. The System consists of three polish platens, each of which is equipped with an optical endpoint detection system. The process consists of three steps with different polish slurries, and is designed to polish copper with a tantalum based barrier, and to achieve good defect performance. Patterned test wafers were processed and characterized to investigate the effect of overpolish, feature size and pattern density. Both electrical testing and various physical measurement techniques have been extensively used for the characterization. It is concluded that dishing and erosion start to develop when the polishing reaches the barrier. The amount of dishing and erosion for each test structure depend primarily on the pattern itself and the amount of overpolishing, and secondarily on CMP consumable and process parameters. Essential to achieve a consistent chip interconnect parametric performance are: an optimized Cu CMP process, a set of interconnect layout design rules compatible with the Cu CMP capability, and equally important or more so, a robust CMP endpoint detection system.

INTRODUCTION

As device scaling continues toward the 0.18 μm technology generation and beyond, device performance will be limited more by the interconnect delay of aluminum metallization than by gate delay. Due to its high conductivity and high resistance to electromigration, copper is the choice of conductor materials for advanced metallization. Damascene is the preferred approach for the fabrication of copper interconnect. A typical Damascene process sequence is shown schematically in Figure 1.

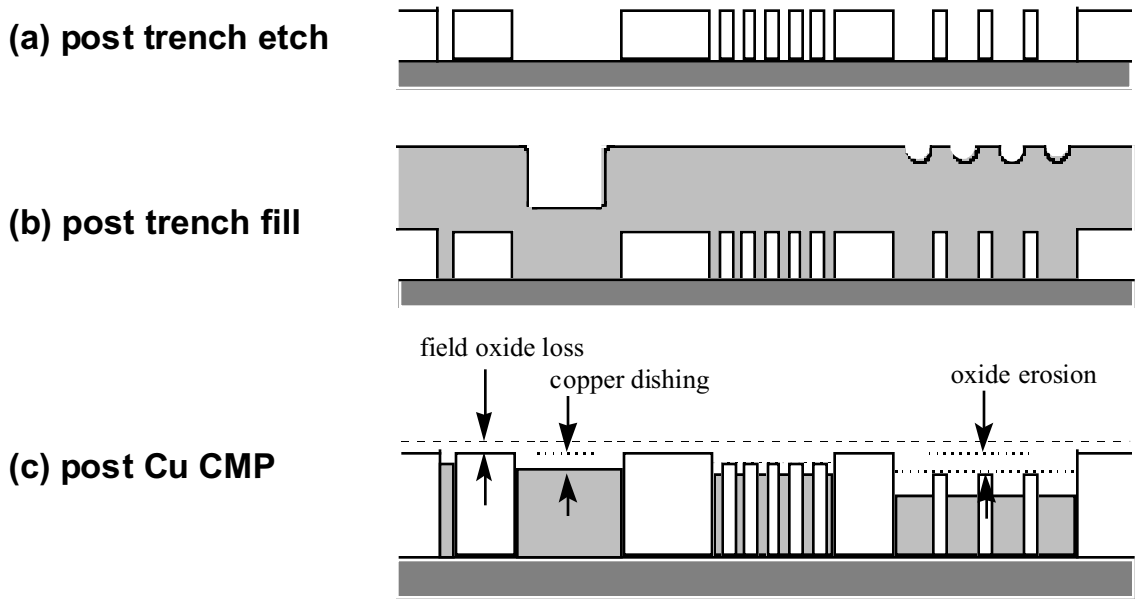


Figure 1. Schematic of the Damascene process sequence

Traditionally, aluminum metallization has been fabricated with a subtractive metal etch process. Factors affecting metal line resistance control include: lithography critical dimension (CD) control,

and metal etch bias and profile control. Metal thickness is solely dictated by the sputter deposition process which typically has excellent uniformity and control. With the Damascene approach, process control of dielectric etch substitutes for that of metal etch. Lithography CD control remains critical. And, Cu CMP evolves as an additional factor, and a very important one, which can substantially affect the electrical line resistance, or the electrical CD (ECD).

A certain amount of overpolish during Cu CMP is required to clear off all surface metal residue between metal patterns and to ensure electrical isolation between neighboring circuits. During overpolish, multiple materials are polished simultaneously, and with different polish rates. This results in copper dishing and oxide erosion which are strongly pattern dependent, as shown in Figure 1(c). Here, oxide is used generically to represent the dielectric material for the copper Damascene interconnect. Field oxide loss is defined as the amount of oxide lost in regions with no metal pattern or very low metal pattern density. This loss is typically small for a well controlled process due to a very high copper to oxide CMP selectivity. With this small field oxide loss accounted for separately, copper dishing and oxide erosion are then defined as the amount of recess of patterned copper or oxide relative to the field oxide surface. Typically, dishing increases with trench width, and erosion increases with pattern density.

EXPERIMENTAL PROCEDURES

Blank test wafers with various film stacks were used for basic process development, polish rate monitoring, and daily process qualification. Detailed process development and characterization were carried out using patterned test wafers with the following two different test mask sets : 1) a dedicated Cu CMP test mask, and 2) a double-level metal test mask set with a comprehensive set of test structures. Most of the test structures on either mask set allow electrical testing and physical metrology characterization.

All copper CMP work has been carried out on a second generation polishing tool, the Mirra® CMP System, which is equipped with three polish platens and an In-Situ-Rate-Monitor® (ISRM). Several formulations of experimental copper polish slurry containing alumina abrasive particles were used. Details of the CMP process development have been presented previously [1]. The ISRM is a laser interferometry based endpoint detection instrument which has been proven to be successful and critical to the required process control for Cu CMP. Details of its underlying theory of operation, system architecture, and experimental results for several representative CMP processes have also been reported previously [2].

EXPERIMENTAL RESULTS ON WIDE TRENCH

In an ideal multilevel copper Damascene process, Cu CMP would remove all overburden copper and result in a perfectly planar surface. The copper thickness inside each trench would be controlled only by the trench depth and line width. In reality, due to the difference in CMP removal rate for different materials, dishing and erosion start to occur when the CMP process reaches the barrier. These dishing and erosion are critical to the Damascene process integration because they create two separate challenges: 1) the copper thickness loss inside trenches affects the electrical line resistance, and 2) the non-planar surface impacts the fabrication of next copper level. As indicated in Figure 1 (c), more pronounced non-planarity typically occurs over (1) wide copper trenches due to dishing, and (2) line and space arrays with high pattern density due to oxide erosion. Therefore, detailed characterization on these two types of test structures is the focus of this investigation.

For dishing of wide copper trenches, characterization was carried out on a 100 μm trench pitch test structure. An optical micrograph of part of this test structure is shown in Figure 2(d). This test structure consists of (1) an array of 100 μm wide trenches separated by 100 μm wide spaces and (2) an isolated 100 μm wide trench adjacent to this array. Test wafers were polished by different amounts of time, and the topography across the 100 μm trench was characterized with a High Resolution Profiler (HRP). The results are shown in Figure 2(a). The polish time of the first polish step is shown as percentage of the required time for CMP to reach the barrier. A short, fix timed

second polish step was then used to remove the barrier. And a third polish step was carried out to ensure good particle performance. The second and third polish steps use different slurries, and both slurries are different from that of the first step. Impact of the second and the third step has been well characterized and is accounted separately for all experiments. All polish time and percent overpolish reported in this work refer to that of the first polish step, which are carefully monitored with the ISRM.

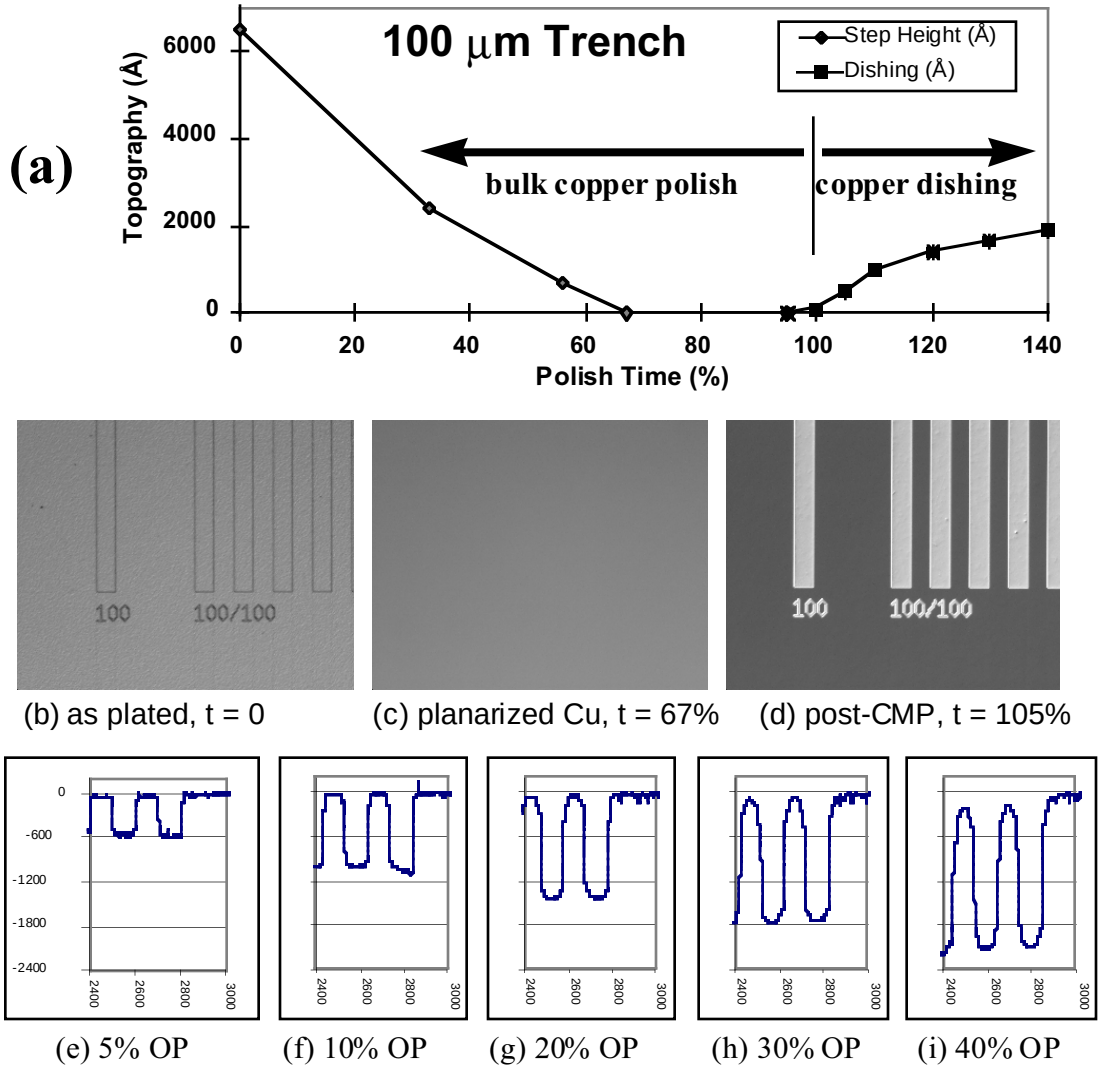
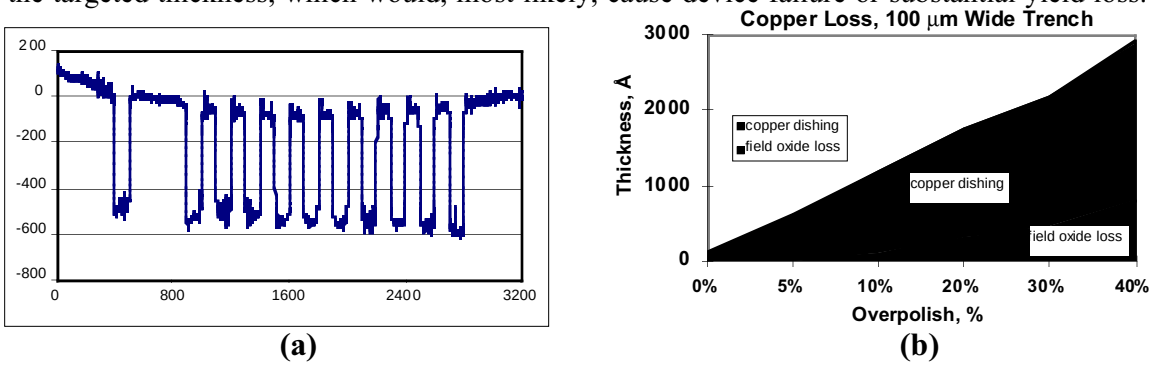


Figure 2. (a) Topography of 100 μm wide trench as a function of CMP time, (b)-(d) optical micrographs of the test structure at different stages of the processing, (e)-(i) detailed HRP profiles as a function of overpolish time, the measured dishing is plotted in (a)

For wafers with less than 100% polish time, the wafer surface was left with full copper coverage. Any measured step height was the remaining step height after partial polish. For wafers with 100% or greater polish time, surface copper was mostly or completely removed The measured step height was then the amount of copper dishing. This measured step height across the 100 μm trench test structure was plotted against polish time, as shown in Figure 2(a). In this specific set of test wafers, approximately 67% of polish time is required to achieve a fully planar surface for this particular test structure, as shown in Figure 2(c). So, the deposited copper thickness potentially could be reduced if this test structure has the slowest planarization rate among all the structure patterns, and if there are no other adverse effects.

After the 100% polish time, dishing is observed to increase monotonically with the overpolish. Two factors dictate the required overpolish: 1) the process uniformity, primarily the thickness uniformity of the deposited copper and the removal rate uniformity of copper by CMP, 2) a CMP system's ability to accurately monitor and control the endpoint. To minimize the effect of process non-uniformity, the deposited copper thickness should be minimized, but it still needs to be sufficient for the specific chip layout and process capability. With good process uniformity, an optimum overpolish results in approx. 500 Å dishing over a 100 μm trench, as shown in Figure 3(a). Separately, field oxide loss was characterized with an accurate optical film thickness measurement tool. Total copper loss for this test structure equals the sum of field oxide loss and copper dishing, as shown in Figure 3 (b). It is observed that a substantial amount of copper thickness loss could occur if the overpolish is not accurately controlled, and copper dishing is the main contributing factor for it in this case. For lower levels of a multi-level copper interconnect, the targeted copper thickness is approximately 5000 Å. The copper loss in a poorly controlled CMP process could easily reach 50% of the targeted thickness, which would, most likely, cause device failure or substantial yield loss.



(a) **(b)**

Figure 3. (a) HRP profile across the 100 μm pitch test structure at optimum overpolish, (b) copper thickness loss for a 100 μm wide line as a function of overpolish

To confirm this observation with electric testing, wafers with van der Pauw test structure were processed with different amounts of overpolish, and tested for sheet resistance. The calculated copper thickness was plotted against the overpolish, as shown in Figure 4(b). The first wafer in this series was intentionally under-polished, and surface barrier residue was observed over the van der Pauw test structure. This renders the electrical testing invalid and results in the wide scatter of the plotted copper thickness. An additional 10% of overpolish in this case resulted in a corresponding copper loss of 1000 Å. To achieve a well controlled interconnect line resistance, the Cu CMP overpolish time would need to be controlled to within a few percent.

EXPERIMENTAL RESULTS ON ARRAYS OF LINE AND SPACE

A variety of line and space array test structures were available on the test wafers for characterization. The 5 μm pitch, 50% density test structure is shown in Figure 5, which consists of a single loop 2.5 μm wide trench separated by a 2.5 μm space, as shown in Figure 5(b); a similar loop with the addition of dummy lines on both sides, as shown in Figure5(c); and an array of similar loops, as shown in Figure 5(d). The loop structures are connected to electrical probe pads for Kelvin resistance measurement. The loop array has an overall width of 2200 μm and length of 2160 μm. There are 15 active loops within the array, equally spaced, which are connected for Kelvin measurement.

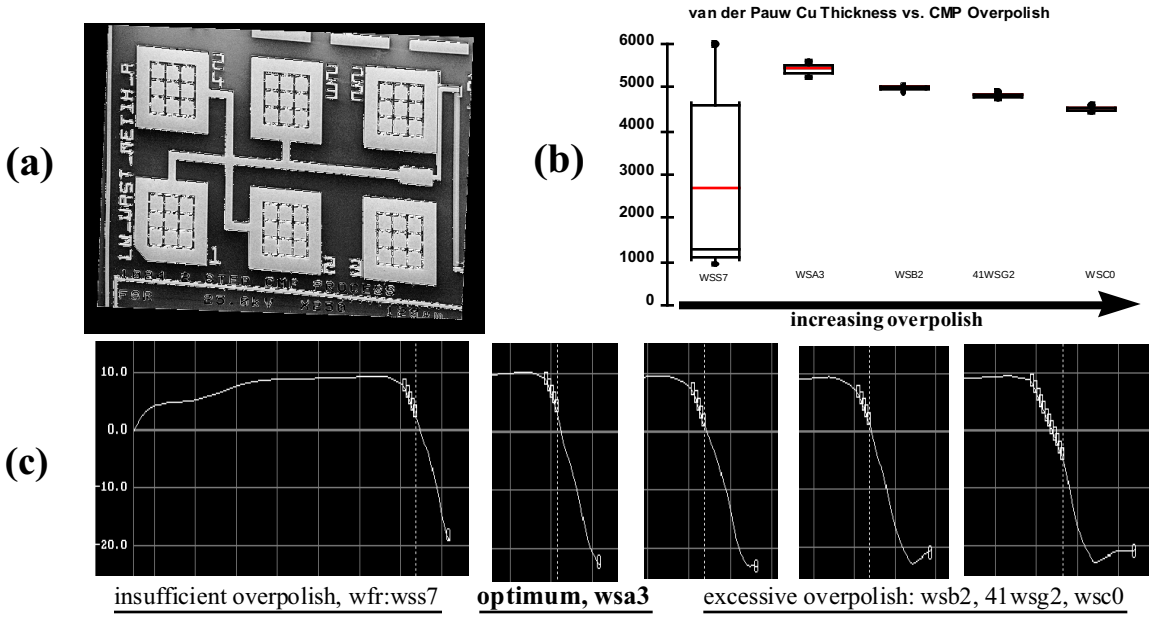


Figure 4. Electrical testing of overpolish, (a) van der Pauw test structure, (b) calculated copper thickness as a function of overpolish, (c) corresponding endpoint curves for the five test wafers

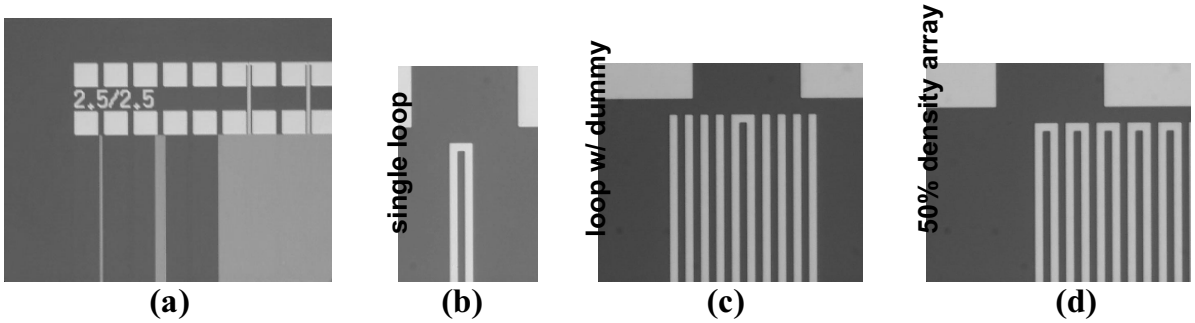


Figure 5. Density test structure of 5 µm pitch, 50% density, (a) overall view, (b)-(d) details of structures

A series of test wafers were polished with different amounts of overpolish for the characterization. Results on the wafer with 30% overpolish are shown as an example in Figure 6. To investigate dishing and erosion in details, the middle portion of the HRP traces is expanded and shown in Figure 7, where zero height represents the field oxide surface.

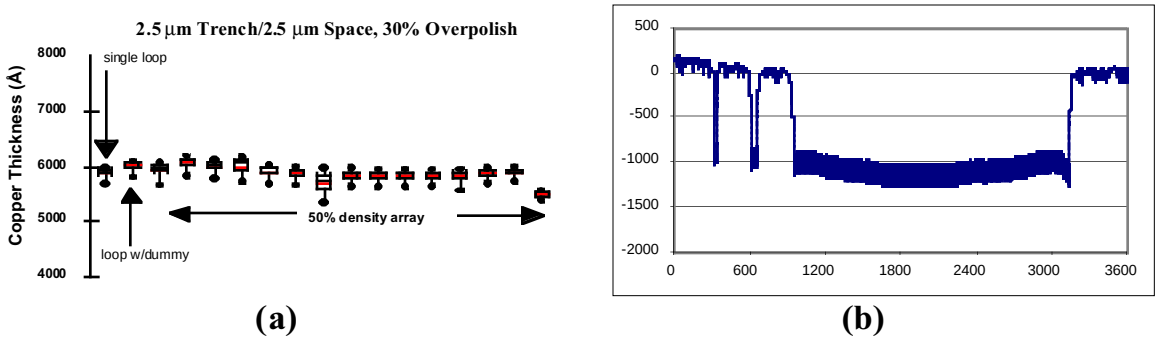
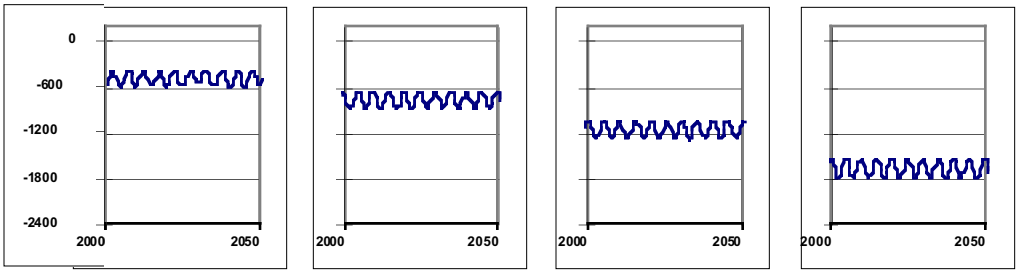


Figure 6. The 5 µm pitch, 50% density test structure with overpolish of 30%, (a) calculated copper thickness from electrical Kelvin measurement, (b) HRP profile across the test structure

Total copper thickness loss for this test structure equals the sum of field oxide loss, oxide erosion, and copper dishing. This is shown as a function of overpolish in Figure 8(a). In this case, the copper dishing reached a constant value quickly after the CMP reached barrier, while oxide erosion continued to increase as the overpolish was increased. This behavior is very similar to what has been observed in tungsten CMP [3].



(a) 10% OP (b) 20% OP (c) 30% OP (d) 40% OP

Figure 7. Details of HRP profile over the middle section of the 5 μm pitch, 50% density line/space array

Similar characterization was carried out over a separate test structure, the 5 μm, 90% density line and space array, on the same test wafers. In this test structure, the linewidth is 4.5 μm and the space separating the lines is 0.5 μm. Results on the wafer with a 40% overpolish are shown in Figure 9. Similar calculation on the total copper loss was carried out and the results are shown in Figure 8(b). As expected, the oxide erosion for the 90% density structure is much higher than the 50% structure, while the copper dishing is smaller. The oxide erosion is the main contributor to the total copper loss, which reaches almost 70% of a nominal 5000 Å thick copper interconnect when a 40% overpolish is used. This observed copper thickness loss behavior over various density structure has been separately confirmed with electrical testing, and very good agreement is observed between the electrical results and physical measurement.

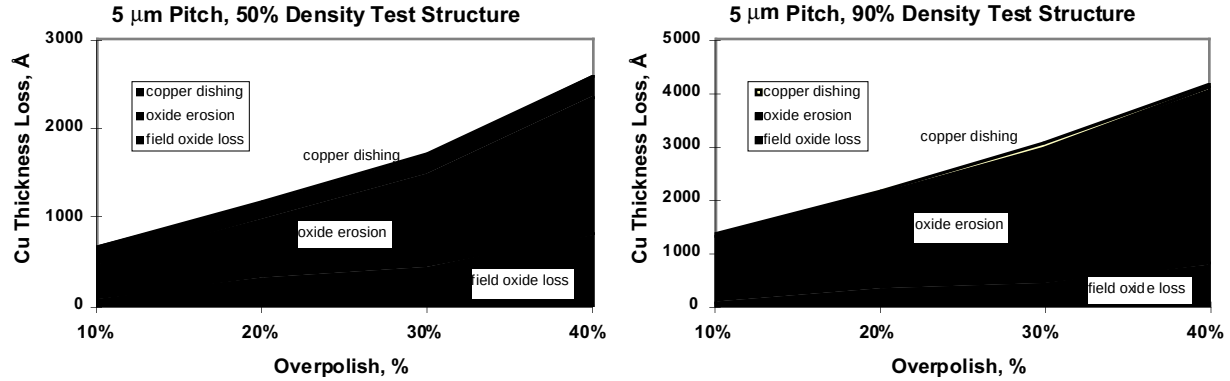


Figure 8. Causes of copper thickness loss on (a) the 5 μm pitch, 50% density test structure, (b) the 5 μm pitch, 90% density test structure

As mentioned earlier, dishing and erosion not only cause copper thickness loss, but also create a non-planar surface which could cause difficulty in the fabrication of next copper interconnect level. This effect is clearly demonstrated with the two optical micrographs shown in Figure 10. In Figure 10(a), the test wafer was polished with excessive overpolish which resulted in substantial dishing over the van der Pauw test structure in metal 1. After metal 2 CMP, surface metal residue was observed over the middle of the van der Pauw structure in metal 1. In comparison, a well controlled metal 1 CMP process resulted in minimum dishing, and no metal residue was observed after metal 2 CMP, as shown in Figure 10(b).

CONCLUSION

A Cu CMP process has been successfully developed on a multi-platen CMP system with the robust endpoint interferometer being the main differentiator to meet the requirement for process control. Patterned test wafers have been processed to characterize the field oxide loss, copper dishing, and oxide erosion, which all contribute to the total copper thickness loss from an ideal Damascene process. Both electrical testing and physical metrology techniques were used for the characterization, and good agreement between them was obtained.

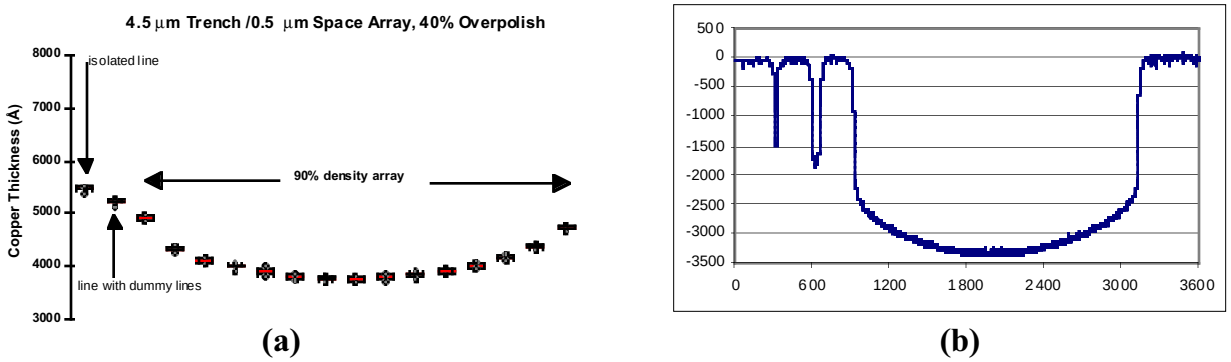


Figure 9. The 5 μm pitch, 90% density test structure with overpolish of 40%, (a) calculated copper thickness from electrical Kelvin measurement, (b) HRP profile across the test structure

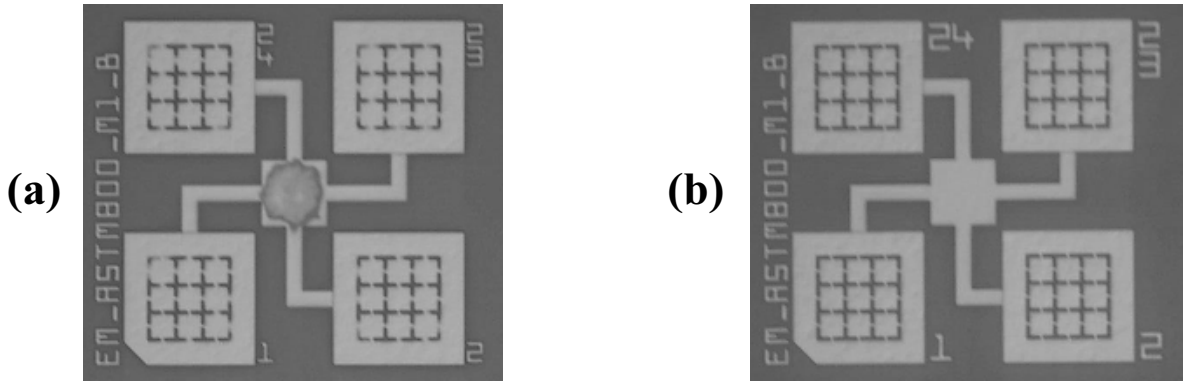


Figure 10. The effect of metal 1-CMP residual surface topography on the Cu CMP of metal 2, (a) surface metal residue as the result of underlying topography, (b) a well controlled process

For wide trenches, copper dishing is the main mechanism for copper thickness loss. For a fine pitch line and space array, oxide erosion is the main contributor to copper thickness loss. For either case, the copper loss increases substantially with increasing overpolish. Therefore, the importance of a robust endpoint instrument and methodology for a successful Cu CMP can not be over emphasized. Through detailed Cu CMP experiments and characterization, one can achieve a comprehensive understanding of the pattern effect for the specific CMP process. One can then define a set of compatible interconnect design rules. With all these combined, a tightly controlled, high yielding copper interconnect Damascene process can be developed and implemented for device fabrication.

REFERENCES

1. Kapila Wijekoon, et al, Proceedings of 1998 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 354 - 363
2. David A. Chan, et al, Proceedings of 1998 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 377 - 384
3. Norbert Elbel, et al, J. Electrochem. Soc., Vol. 145, No. 5, May 1998, pp. 1659 - 1664