

Comparison of Oxide Planarization Pattern Dependencies between Two Different CMP Tools Using Statistical Metrology

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EXECUTIVE SUMMARY

This paper examines the oxide planarization pattern dependencies between two different commercial CMP tools. A statistical metrology framework has been used to separate variation into wafer- and die-level components. We find that die-level layout pattern dependencies are very similar, even though wafer-level nonuniformities may differ greatly.

INTRODUCTION

Chemical-Mechanical Polishing (CMP) is emerging as a leading technology and method of choice for solving the problems of dielectric planarization. CMP is widely used in advanced IC development and manufacturing to achieve a high degree of global planarization. However, it has been established that CMP remains hampered by systematic and random inter-level dielectric (ILD) thickness variation at the wafer- and die-level [1, 2]. Pattern dependencies within the die, in particular, have been of concern for both manufacturability and product design. Common pattern signatures for the local ILD variations in removal and planarization rate have been reported [3]. However, the role of different polishing tools in layout patterns has not been investigated.

In this paper we utilize a statistical metrology framework [1, 4] to study the intra-die ILD thickness variation due to underlying patterns between two different CMP polishing tools. Since the wafer and die-level sources are deeply confounded, it is difficult to characterize the tool dependencies until these sources are decomposed. After application of variation decomposition techniques, the die-level variation can be analyzed for its pattern dependencies. We have shown that for similar polishing pad and processing conditions (e.g. platen speed, back/head pressure and spindle speed) between the two tools, the die-level variation is similar and is fundamentally dependent upon the underlying topographies while a substantial wafer-level variation results.

STATISTICAL METROLOGY EXPERIMENT

Statistical metrology is a methodology for the systematic assessment and quantification of the sources of variation in a given semiconductor manufacturing process. The methodology requires a large number of measurements for statistical modeling. It also emphasizes the design of experiments to develop electrical test structures, use of short flow processes to ensure minimum variation in the final parameter from the confounding interactions between processing steps, and close coupling to TCAD tools necessary for extracting the desired parameters from electrical measurements.

The test structure used in this experiment is a metal-to-metal capacitor to infer the ILD thickness as shown in Figure 1a. The capacitor test structure has a uniform top electrode and bottom electrode consisting of various combinations of layout factors such as line width and spacing, finger length, the number of fingers, geometric orientation and presence or absence of an interaction ring around the structure (Figure 1b). Combinations of six layout factors form a half-fractional factorial experiment yielding 32 unique structures. Four structures are put together in a subdie layout shown in Figure 2 with corresponding resistive structures to account for local line width variation. The subdie layout is replicated four times within the die to obtain spatial mapping. Figure 3 shows the 1.45cm x 1.45cm short-loop test die. The fourth quarter of the die also includes large uniform density intensive structures to study the area dependence but also serve as dense patterns in the die.

Test wafers were processed in a short-flow Metal1-Metal2 process [1], with half of the wafers being polished on commercial tool A and the other half on commercial tool B. Slightly different slurries and pad conditioning techniques were used but the polishing pads, back/head pressure, platen speed, and spindle speed were similar on the tools. The ILD thickness data were extracted from AC high frequency (100 kHz) capacitance measurements [1].

RESULTS AND DISCUSSION

The ILD thickness variation sources can be categorized into wafer-level, die-level, die and wafer interaction, and residual terms. The wafer-level variation is often caused by process perturbation and drifts in equipment and consumables and is relatively invariant of pattern density and other layout effects. On the other hand, the die-level variation is attributed to the layout patterns within a die. Statistical methods were used to separate these two components [5]. Figure 4 and 5 depict the wafer-level variation extracted from a typical wafer polished on tool A and on tool B respectively. The effect of wafer edge and flats can be discerned from these figures. Both tools exhibit substantial wafer-level (or inter-die) variation. These results are quite striking given that all the wafers from one lot were fabricated using the same deposition process. Clearly, the equipment factors, different pad conditioning techniques, slurry distribution and other macroscopic physical effects during polish contribute to this wafer-level nonuniformity.

Figures 6 and 7 show the die-level variation held common between all dies on the wafer. The die-level (or intra-die) ILD thickness variation pattern is found to be nearly identical. Both tools exhibit a similar pattern “signature” at the die-level with the primary difference being relative attenuation in the magnitude of the variation. We attribute most of this attenuation to a difference in the total thickness of oxide removed. The denser structures on the fourth quarter of the die have less variation and are polished slower compared to the rest of the features. These results indicate that feature/pattern scale variation appears to be largely determined by pad and layout characteristics and are only weakly impacted by process conditions.

Figure 8 shows a quantitative comparison of extracted die-level variation components for tool A versus tool B. The correlation coefficient for tool A versus tool B is 97%, and the magnitude of the slope indicates the difference in attenuation of the variation. A qq-norm plot also revealed that the residuals from the linear fit shown in Figure 8 are normally distributed.

IMPACT

The experimental results presented in this paper provide clear evidence that different physical effects are at work at the wafer and die-levels. We believe that the methods presented here can be used to study the effect of different process flows and equipment drift and replacement on both die-level and wafer-level variation. The explicit decomposition and modeling of wafer- and die-level variation, especially across different tools and consumable sets, can be extremely useful as part of a program to reduce pattern-sensitive effects in CMP.

ACKNOWLEDGEMENTS

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Figure 1. Capacitance Test Structures

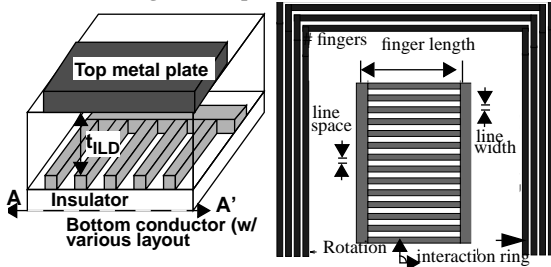


Figure 2. Probe Layout

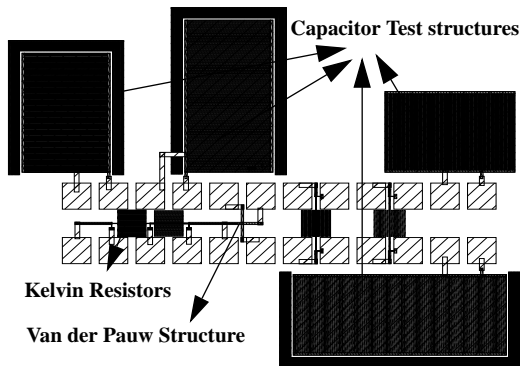


Figure 3. CMP/ILD Thickness Die Layout

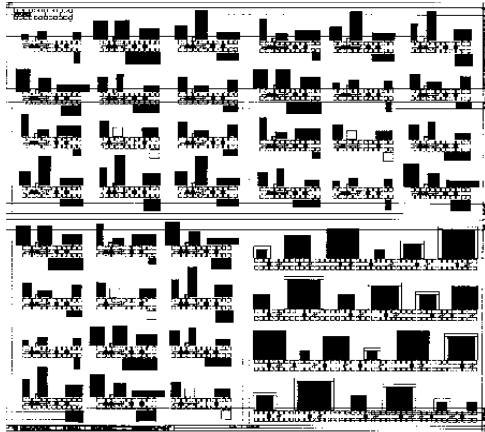


Figure 4. Wafer-Level Variation for Tool A

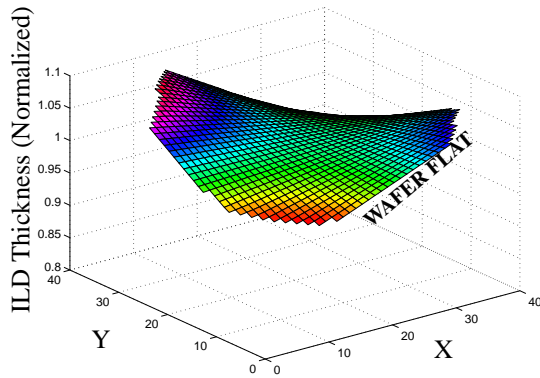


Figure 5. Wafer-Level Variation for Tool B

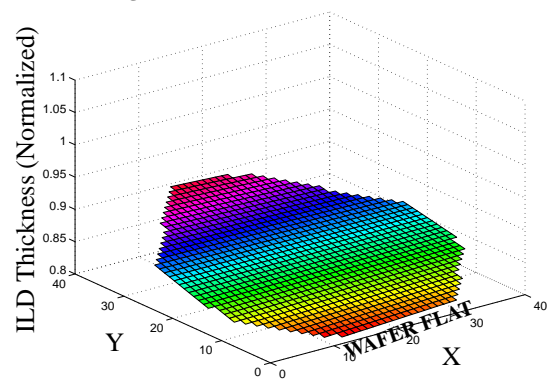


Figure 6. Die-Level Variation for Tool A

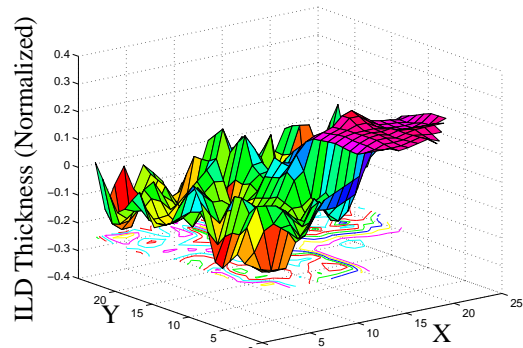


Figure 7. Die-Level Variation for Tool B

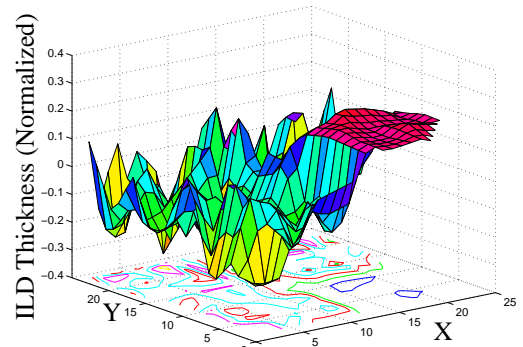


Figure 8. Quantitative Comparison of Die-level variation for Tools A and B

