Assessing and Characterizing Inter- and Intra-die Variation Using a Statistical Metrology Framework: A CMP Case Study

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ABSTRACT

A statistical metrology methodology has been developed and used to study the contributions to spatial variation in ILD thickness remaining after chemical-mechanical polishing. New elements of statistical metrology are described, including a three-phase experimental approach and the use of a modified repeated measure analysis of variance technique.

INTRODUCTION

As device dimensions continue to shrink below half micron dimensions and the demand for both yield and performance rises, the assessment and control of process and device variation becomes critical. Yield loss from parametric sources will rise unless process margins are characterized to a higher degree than currently available [1].

Process and device variation in VLSI manufacturing occurs with different scope and extent. Process perturbation, drifts, and equipment factors result in lot-to-lot variation, while within-wafer variation may stem from process non-uniformities. While substantial work has focused on the control of lot and wafer-level variation [2], die-level variation has received little attention despite the potential impact on circuit performance [3]. This spatial variation has both systematic and random components. Currently, device variation is often lumped into a single large distribution as part of a "worst-case" approach to modeling. A methodology is needed to transform this large distribution into deterministic components that can be compensated or designed around.

We present statistical metrology as a methodology to assess variation and parameterize any resulting circuit and process impact. Variation assessment is achieved by identifying and explicitly modeling the individual sources of variation. The resulting quantification of variation components enables better process modeling, facilitates process control, and provides realistic data for statistical circuit modeling.

In this paper we use statistical metrology methods to study inter-level dielectric (ILD) thickness variation for two representative chemical-mechanical polishing (CMP) processes. We suggest that three phases of experimental design are appropriate to (1) identify important factors; (2) construct explicit variation models, and (3) quantify the impact of variation in realistic chip environments. We present a case study in which these phases as well as new modeling methods, in particular a modified form of repeated measure ANOVA (Analysis of Variance), are used to model die- and wafer-level variation for representative CMP/ILD processes.

STATISTICAL METROLOGY METHODOLOGY

Statistical metrology can be used in three phases of inter-linked statistical experiments as shown in Fig. 1. First, a screening experiment explores a large space of possible layout or process factors that potentially affect a particular device parameter. This experiment entails identification of the key factors that affect the parameter of interest. Second, a model generation experiment uses additional levels for identified key factors to build semi-empirical models of parameter variation. Third, a "domain specific" or environmental experiment can be designed to mimic real products such as a test design which focuses on the factor levels that typically arise in microprocessor design.

Key elements of statistical metrology include: development of optical or electrical test structures to gather the volume of data necessary for statistical modeling; the use of short flow processes to ensure minimum variation in the final parameter from confounding interactions between processing steps; and close coupling to TCAD tools necessary for extracting desired parameters from electrical or optical measurements.

CMP CASE STUDY

ILD thickness is an important parameter: thickness variation impacts interconnect capacitance and can result in degraded or spurious circuit performance (e.g. clock skew). Because advanced technologies will require intensive use of CMP for dielectric planarization [5], and CMP of ILD is known to suffer from systematic and random ILD thickness variation at the wafer and die-levels [4, 7], representative CMP processes are the focus of this case study.

Previously, we reported a first phase screening experiment to understand ILD thickness variation in a representative CMP process [4]. After briefly summarizing and extending that work, we present a second experiment in which we model in more detail the interaction distance between dense layout blocks, as well as more closely mimic a typical circuit environment.

A large number of measurements are needed to extract and quantify both within-wafer and intra-die variation. A test structure consisting of a metal-to-metal capacitor structure was used to infer the ILD thickness. The capacitor test structure has a bottom electrode consisting of various combinations of layout factors such as line width and spacing, finger length, the number of fingers, geometric orientation, and the presence or absence of an electrically floating interaction ring. The top electrode is a uniform metal layer covering the entire structure [4]. The short flow process used for both

cases is a three mask CMP process. The ILD data was inferred from high frequency AC (100 kHz) capacitance and line width measurements and TCAD simulations [4]. In this paper, all data has been normalized by an arbitrary constant.

The wafer- and die-level variation is identified using the variation decomposition analysis shown in Fig. 2. The decomposition algorithm assumes an additive model where total variation is expressed as the sum of die-level variation, wafer-level variation, the confounding of die- and wafer-level variation, and any remaining variation which is assumed to be random (Fig. 3).

The wafer-level estimator is generated using a regression based approach while the die-level variation is extracted using a modified form of repeated measure ANOVA. In this technique, a standard ANOVA model is first computed for each measured die, and then an average ANOVA model is formulated and used to estimate the die-level variation (Fig. 4). These methods will be described in detail elsewhere [6].

CMP STUDY #1: SCREENING EXPERIMENT

The short-loop test die used for this screening experiment is shown in Fig. 5. A half-fractional factorial design of experiment on six layout factors resulted in 33 unique structures (including a center-point structure). Each structure was replicated four times and randomly distributed within each die. Additional area intensive structures were included in the fourth quad of the die to probe area dependence often associated with CMP processes [8].

Fig. 6 shows the systematic wafer-level variation across the wafer. The wafer-level variation is piece-wise smooth and low frequency and is invariant of die patterns. Such shapes are often attributed to consumable and equipment issues. On the other hand, the die-level variation shown in Fig. 7 is associated with layout features and patterns dependencies.

Using the repeated measure ANOVA technique, the contributions of ILD thickness variation due to the layout factors within each die are examined. The ANOVA results indicate that the interactions of finger length and number of fingers as well as the interaction between line width and spacing are the most significant [4]. To facilitate physical understanding, the original factors are re-mapped into local area and density for each structure. A model based on these factors explains the ILD thickness variation well as shown in Fig. 8.

Fig. 9 shows the scatter plot of normalized ILD thickness versus area for different densities on a particular die. The figure hints at some of the complex effects manifested in CMP processes such as pad bridging which may occur for structures with different densities and areas [6].

CMP STUDY #2: ENVIRONMENTAL/MODELING EXPERIMENT

This experiment evolved from the previous CMP screening experiment. The new design mimics the environment present in a typical ASIC chip as well as studies the effect of interaction distance [7]. A full-factorial design on five factors (line width and spacing, finger length, the number of fingers, and geometric orientation) in combination with four levels of a new interaction distance layout factor yields 129 unique structures (including several center-point structures). Fig. 10 shows the layout of the short-loop test die. Additional test structures including area intensive structures with and without dummy fill environment are also included to study the effect of dummy lines on ILD thickness [7].

The raw ILD data was decomposed into its variation components using the method highlighted in Fig. 2. The resulting wafer-level variation and die-level variation are shown in Figs. 11 and 12. The wafer-flat can be clearly discerned, and the feature and pattern dependency on the die-level variation is quite prominent especially for some of the more dense structures in the upper right region of the die.

The pattern contributions from the die-level variation are analyzed using the repeated measure ANOVA technique, which identifies line width, line spacing, and interaction distance as the primary factors. A scatter plot of the fitted model versus the raw data is shown in Fig. 13. A relatively good fit is obtained despite the presence of several outliers. Fig. 14 highlights the effect of density, pitch, and interaction distance on the ILD thickness. From this figure, we can infer that complex interactions between pitch, density, and interaction distance are causing significant ILD thickness variation despite the inclusion of dummy structures.

CONCLUSION

In this paper, a statistical metrology framework was used to understand and model CMP ILD thickness variation via the use of screening and environmental/modeling experiments. In each case, the complex interactions between designed layout factors such as pitch, density, area, and interaction distance and ILD thickness were observed. From these results, we conclude that more extensive mask designs will be needed to model and understand ILD thickness variation remaining after CMP planarization.

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